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TSV-to-TSV Resistive Bridging Defects Post-Bond Testing and Diagnosis

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Abstract

Through Silicon Vias (TSVs) defects are a serious concern for the reliability and the yield of three dimensional integrated circuits (3D ICs). In this paper, a post-bond, parallel testing and diagnosis scheme is proposed, for the detection and location of resistive bridging defects between TSVs. This scheme is based on an all-digital built-in testing circuitry. Monte-Carlo analysis results, using the statistical models of the 90nm technology of UMC, are presented to validate the new testing approach. In addition, comparisons with the most advanced testing technique in the literature, for TSV bridging defects, accentuated that the proposed scheme is more efficient in terms of defect detection effectiveness, robustness, tolerance, cost and design for testability effort.

1. Introduction

Three dimensional integrated circuits (3D ICs) are the main vehicle to overcome the limitations of Moor's law due to their higher speed performance, lower power consumption and reduced costs [1]. A key technology among other to support 3D integration is the through-silicon via (TSV) interconnects. TSVs are used to connect different dies in 3D ICs [2], providing higher density and low-capacity interconnects compared to traditional wire-bonds [3].

TSVs, are used to connect different dies (tiers) in a three- dimensional integrated circuit. The fabrication of these structures is prone to defects that affect the reliable operation of 3D ICs. Voids and cracks are often formed in TSVs [4]- [6], due to thermal and mechanical stress on the wafer or during the bonding process of the dies in a 3D IC as well as improper metal filling of the TSV tube. Moreover, impurities in the surrounding oxide of the TSV, formed during fabrication, may create a short between the TSV and the grounded substrate [7]. In addition, due to the continuous shrinkage of the TSV-to-TSV pitch as well as of the bumps spacing [8], [9], the probability of bridging defects between TSVs [10] is increased over the years [11]. All above mechanisms may result to weak defects that are difficult to be detected. Such defects will affect the signal quality in 3D ICs.

TSV testing is performed a) before the die bonding (pre- bond test) in order to detect die fabrication defects [12], [13] and b) after the bonding of the dies (post-bond test) [14] in order to detect bonding process defects along with die fabrication defects and improve the product yield [15].

Various post-bond TSV testing methods for resistive open defects have been proposed in the literature, like in [12], [15], [16], [17], [18] and [19]. In [20] a crosstalk testing scheme for the detection of interference between TSVs is proposed. Testing issues for TSV-to-TSV bridging defects are explored in [11], [21], [22] and [23]. The authors in [21] consider the wired-OR and wired-AND models for the bridging defects detection using simple digital logic. However, these models are not quite effective for the detection of weak defects. In [22] a pair of analog comparators is exploited for the comparison of the TSV voltage with a reference voltage in order to detect bridging defects between TSVs. Next, in [23] a voltage divider structure is exploited for bridging defects detection. According to this approach, in a TSV array analog comparators, one in each row and column, compare the dividers' voltage levels with reference voltage levels for defect detection. An advanced testing technique for bridging defects between TSVs is proposed in [11]. Pairs of adjacent TSVs form voltage dividers when an in-between bridging defect is present. An analog comparator is used to compare the divider output with a reference voltage. This approach provides parallel TSV testing capabilities and a good bridging defect resistance resolution. However, in all three techniques above ([11], [22] and [23]) analog comparators are employed, that are affected by process variations, increase the design for testability effort and require the existence of one or more voltage references. In this paper, a post-bond built-in test and diagnosis technique is presented for the detection of resistive TSV-to- TSV bridging defects, which is based on the testing scheme earlier proposed by authors of this work for TSV resistive open and TSV-to-Substrate short defects [19]. The propagation delay between the output signals of two TSVs that are fed by complementary pulse signals is used to determine whether a defect is present or not. The advantages of the proposed solution are:

- It is based on an all-digital, built-in, circuit.
- It is robust and provides tolerance over process and temperature variations that may affect the testing circuitry.
- It is a low-cost technique (with respect to silicon area and design effort), through which all TSVs can be tested in parallel.

The rest of the paper is organized as follows. The TSV model is presented in Section 2. Section 3 introduces the proposed post-bond TSV testing technique and analyzes the operation of the corresponding test circuitry. Section 4 presents simulation results that consider process and mismatch variations, through Monte-Carlo analysis, on a design of the proposed TSV testing circuitry in the 90nm technology of UMC. These results validate the effectiveness of the proposed scheme. Moreover, comparisons of the proposed testing scheme with the most advanced and recent TSV testing technique in [11] are also discussed. Finally, conclusions are presented in Section 5.

2. TSV model

The lumped element model presented in Fig. 1 describes the electrical behavior of a TSV [24]. The resistance RTSV is few Ohms, the inductance LTSV is a few pH and the capacitance CTSV is several fF. In lower and middle frequencies, the inductance components has low impact in the electrical behavior of the TSV. In this study the full RLC model is used to increase the accuracy of the simulation results.

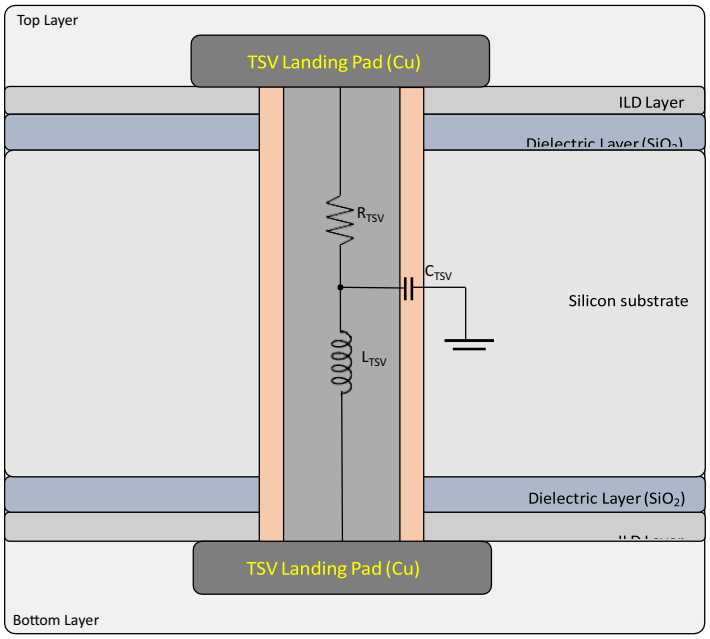

Figure 1: TSV lumped element model.

The geometry, materials and fabrication parameters of a TSV affect the parameters of the TSV lumped element model. The values of the CTSV and LTSV are given in (1) and (2) respectively [25].

$$C_{TSV} = \frac{2\pi\varepsilon_{r,ox}\varepsilon_0 h_{TSV}}{\ln\left(\frac{r_{TSV}+t_{ox}}{r_{TSV}}\right)} \quad (1)$$

$$L_{TSV} = \frac{\mu_0 h_{tsv}}{2\pi}\left[\ln\left(\frac{2h_{tsv}}{r_{TSV}}\right) - \frac{3}{4}\right] \quad (2)$$

For a TSV its height may range from 5μm to above 100μm and its diameter from 1μm to above 10μm, with aspect ratio 20:1 or lower [9]. The adopted parameters of the TSV structure [9] are shown in Table 1, leading to the following approximate values for the TSV model: RTSV = 50 Ohms CTSV=10fF and LTSV=4.5pH. It should be noted that there are more detailed models than this one. However, this is the most commonly used for simulation purposes. Due to the large dimensions of a TSV, its process variability is expected to have negligible effect on its performance. So, for the passive elements of the TSV model, simple Virtuoso models from the analog library were used. On the contrary, process and mismatch variations for the components of the rest circuitry were considered, leveraging UMC 90nm Monte Carlo models.

Parameter	**TSV structure simulation values**	
	Description	***Value***
hTSV	TSV height	10 μm
rTSV	TSV radius	1 μm
tox	Insulator thickness	0.25 μm
εr,ox	Relative permittivity SiO_2	3.9
ε0	Vacuum permittivity	$8.85\ 10^{-12}$ F/m
μ0	Vacuum permeability	$4\pi\ 10^{-7}$ H/m

Table 1. Parameters of the considered TSVs

3. The Proposed TSV Testing Scheme

In order to achieve the parallel testing of multiple TSVs and identify the pair of TSVs with the in between resistive bridging defect, we propose the following test scheme as shown in Fig. 2. A multiplexer (MUX) is placed at the input of each TSV to support the normal and test modes of operation. One input of the MUX is fed by the functional data (Dataj) and the other by the test signal (Test_Pulse). The test signal is a pulse that is generated by a simple Pulse Generator. Alternatively, the system clock signal can be used. Each TSV and two of its adjacent (immediate neighboring) TSVs form two pairs of conjugate TSVs. In a pair of conjugate TSVs, one TSV is fed by the test signal and the other is fed by the complement of the test signal. During the test procedure, a Controller (Tester-ATE or Built-In Self Test (BIST) circuit) activates the Test_Enable signal that controls the multiplexers. When the Test_Enable is high the test signal (or its complement) feeds the TSV. The outputs of a pair of conjugate TSVs drive a XNOR gate. Thus, each TSV feeds a pair of XNOR gates, these related to its conjugate TSVs. Finally, the output of each XNOR gate feeds a scan flip-flop (SFF) in a scan chain.

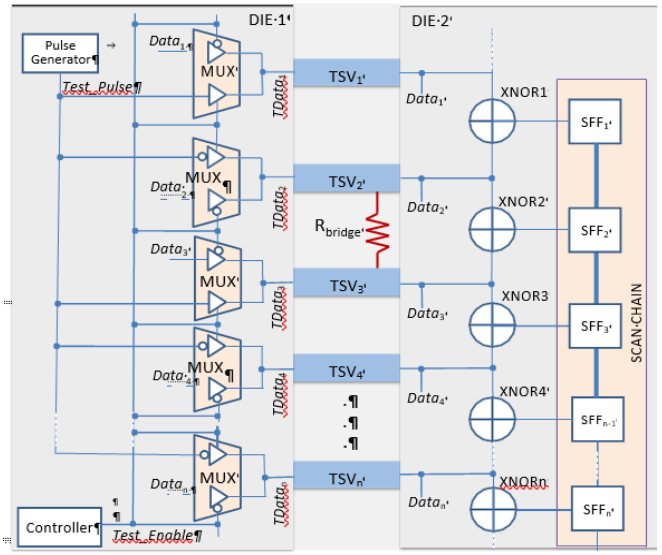

Figure 2: The proposed scheme for the parallel testing and diagnosis of multiple TSVs for bridging defects

During the test mode, the signals that are propagated to conjugate TSVs are complementary and therefore in the defect-free case the output of all XNOR gates is at logic low. In the case there is a resistive bridging defect between a pair of conjugate TSVs, e.g TSV2 and TSV3, then it is expected that the test signal propagation delay on these two TSVs will be different with respect to their adjacent, conjugate, TSVs (TSV1 and TSV4 respectively). As a result a high pulse is expected at the output of the pertinent XNOR gates. The duration of this pulse depends on the relative delay of the signals, which essentially reflects how severe is the defect. Fig 3 shows the structure of the scan cell and the detailed topology of the scan chain. The input D of the flip-flop is always at logic high (VDD). The clock input CK of the scan cell is driven through a multiplexer either from the system clock signal or from the output of the XNOR gate. The multiplexer is controlled by the scan enable signal (SE), thus during the test phase we have two modes of operation. Capture mode. In this mode test data capture occurs. The scan enable signal is set to low (SE='0') and thus the input D (that is permanently set to VDD) is selected to feed the scan flip-flop (SFF) while the XNOR gate drives the clock input CK of SFF. In case that a high pulse triggers the input CK, which corresponds to the detection of a TSV defect, the output of the SFF is set to high. Consequently,

the detection of the defects is asynchronous and independent of the Pulse Generator signal or the system clock, providing better detection capability of minor defects. Scan mode. During the scan mode, the scan enable signal is set to high (SE='1'), therefore the SIN input is selected to feed the SFF while the clock signal CLK drives the clock input of the SFF. A scan-out operation is performed with successive pulses of the CLK signal in order to collect the test data from the scan chain. In parallel, since the SIN input of the first scan cell at the top is permanently set to zero (GND) the scan chain is initialized to the all zero state. In test mode, initially, all scan cells must pre-set to the all zero state, so that a dummy scan-out operation is performed to initialize the scan chain. After capturing the test response in the scan chain, a new scan-out operation is applied to extract the test data in order to detect and locate possibly defective TSVs. The scan mode of operation is a typical and fully compatible scan operation as these used in today ICs.

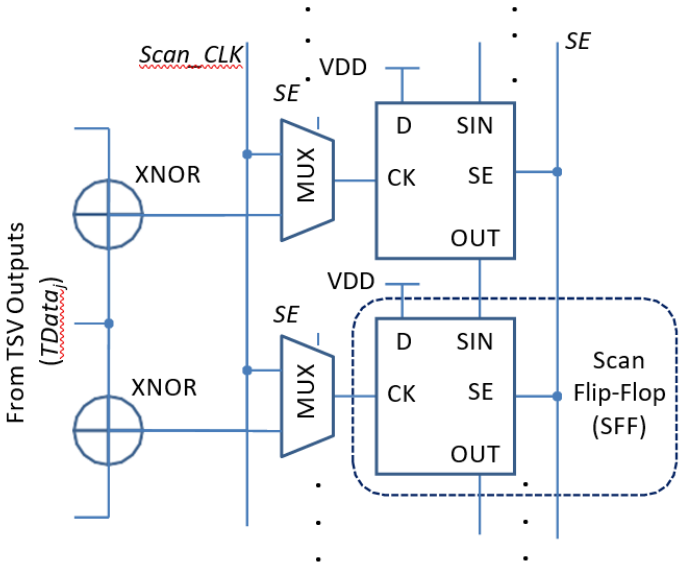

Figure 3: A detailed view of the scan chain structure.

Note that the position of high values in the test data of the scan chain indicates the presence of defective TSVs. Specifically, a scan cell that captures a high value indicates that at least one of the two TSVs that feed it is defective. Consequently, either a bridging defect is between the two TSVs that drive the scan cell or a bridging defect is between one of the TSVs that drive the scan cell and a neighboring TSV.

An important issue that should be addressed is the simultaneous propagation of the test pulse (Test_Pulse) from the Pulse Generator to the MUX array and the test signal (TDataj) from the MUX output, through the pertinent TSV, to the inputs of the corresponding XNOR gates, aiming to avoid any skew. So in order to eliminate this skew, an appropriate routing of the Test_Pulse and TDataj signals is required. In Fig 4, an indicative routing of the TDataj signal is presented. In this way, possible skew issues, due to process variations, will be negligible.

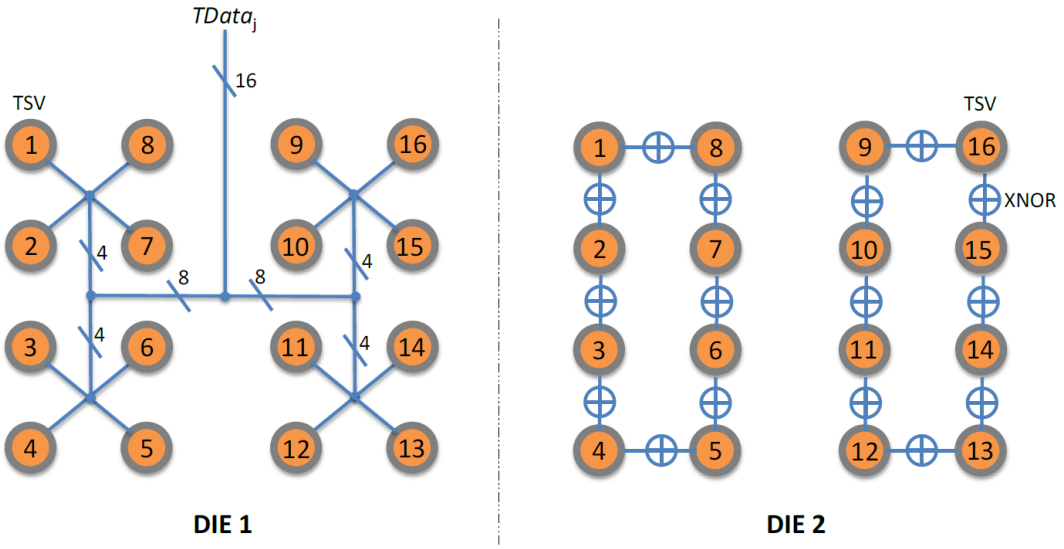

Figure 4: Indicative TSV layout and signal routing in a cluster of 16 TSVs. Each TSV number indicates a TSV that starts at DIE-1 and ends at DIE-2.

4. Simulation Results

For the validation of the proposed test and diagnosis scheme, an array of four TSVs, according to Fig. 2, was designed and simulated at the Cadence environment (Virtuoso, Spectre), using the model files of the UMC 90nm technology. The testing structure incudes the MUXes, the XNOR gates, the SFFs, as well as the defect free model of the TSV and a bridging defect between two TSVs, which is modeled as a resistance between TSV2 and TSV3 (RBridge in Fig. 2). For the TSV model indicative values for the pertinent components were used (RTSV = 50 Ohms, LTSV = 4.5pH and CTSV = 10fF). In addition, the signal interconnects were modeled with a resistance, exploiting the RNNPO_RF resistance model, which is provided by UMC, aiming to be able to perform statistical (Monte Carlo) simulations which also take into account wire process variations that may accentuate possible signal propagation skew issues. Due to the large dimensions of a TSV, process variations effects on this component are expected to be negligible.

4.1 Typical Conditions

In Fig. 5, simulation results from a defect free TSV are presented. All XNOR outputs are permanently low indicating no defect detection. Next, the presence of a hard bridging defect between the two TSVs, leads the output of at least on XNOR gate to generate a high pulse that triggers the pertinent SFF. Thus, the defect is detected. In Fig. 6, simulation results from a defective case are presented. A bridging defect of 3KOhms is set and the test result is the generation of a robust pulse at the output of the second XNOR gate (XNOR2).

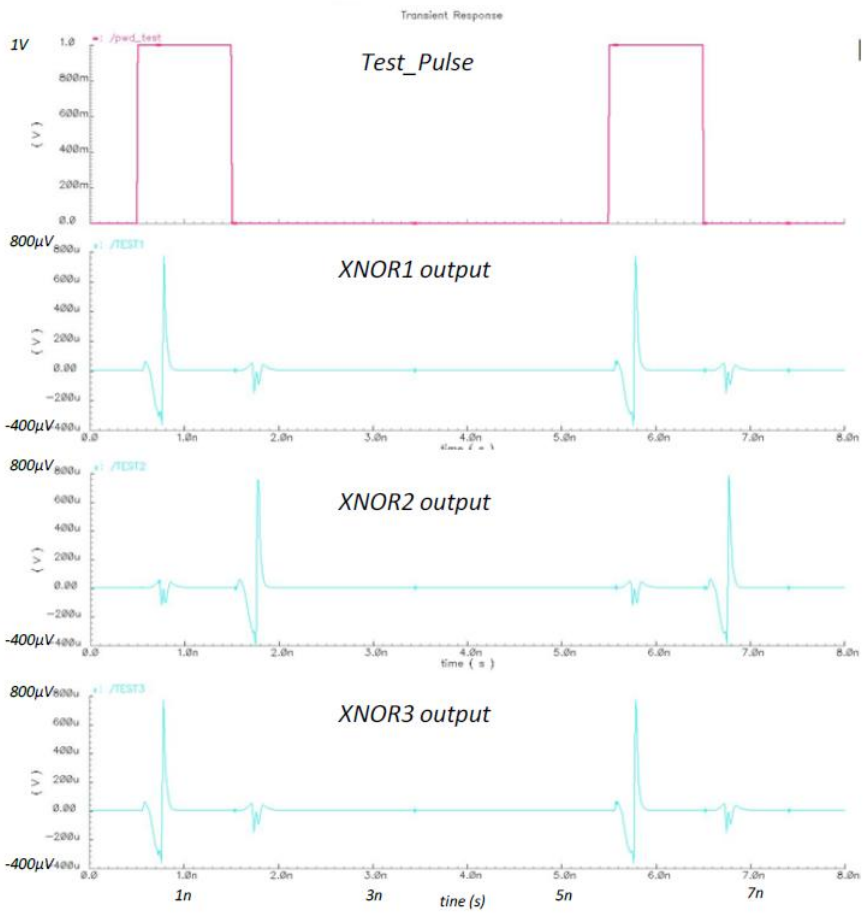

Figure 5: Simulation results for the defect free case (RBridge = ∞). No defect detection indication at the outputs of the pertinent XNOR gates.

However, as the resistance of the bridging defect increases, the width and the amplitude of the pulse generated by the corresponding XNOR gate tend to decrease. As a result, above a maximum resistance value, the generated pulse will not trigger the SFF cell and the defect will not be detected. In this work, we adopted severe specs for the characterization of a pulse generated by a XNOR gate as robust; that is, the pulse amplitude must be at least 90% of the power supply voltage VDD and its width must be at least the minimum hold time of an SFF cell (thold = 100ps). The above minimum acceptable amplitude and width are required for the proper triggering of the SFF and the detection of the bridging defect. As we can see for the case of the bridging defect in Fig. 6, with the resistance value at 3KOhm, the output of XNOR2 provides a robust pulse, according to the above restrictions, for the triggering of the corresponding SFF cell. In the same figure, the pulses generated by XNOR1 and XNOR3 are not compliant with the above limitations (these are not robust pulses) and will not contribute to the defect detection. For the typical process corners the maximum detectable bridging defect resistance (a resistance for which a robust pulse is generated) is equal to 3.2KOhm.

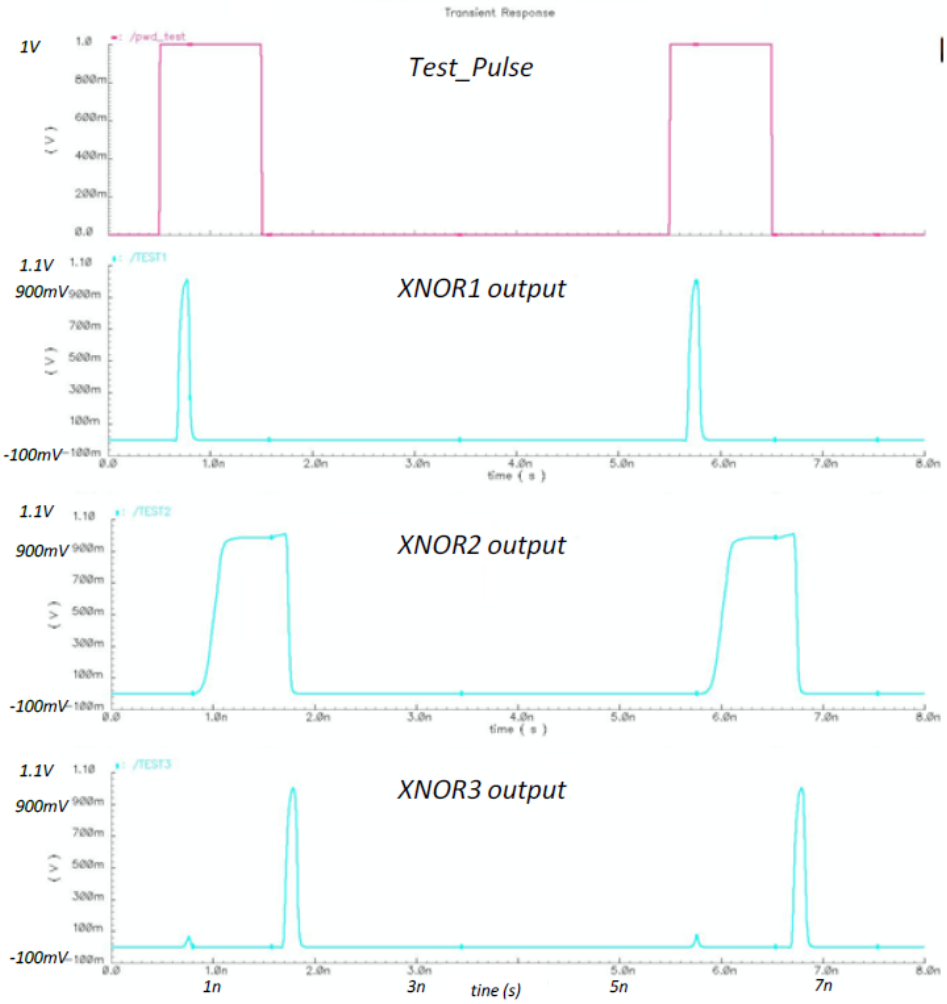

Figure 6: Simulation results for a defective case (R_{Bridge} = 3KOhm). The output of the second XNOR gate provides a robust pulse for triggering the SFF.

4.2 Monte-Carlo Analysis

Monte Carlo analysis, by considering process and mismatch variations, was performed on the proposed testing scheme in Fig. 2, using the statistical device models of the UMC 90nm technology. In this analysis we consider variations of the active devices as well as variations on the signal interconnects, aiming to explore the detection efficiency of the proposed scheme. 1000 runs are applied in each case. In the defect free case, no defect detection indication is generated by the XNOR gates in all Monte Carlo (MC) runs, as it is shown in Fig. 7.

According to the MC analysis, in the presence of a bridging defect the proposed TSV testing and diagnosis scheme is capable to detect and locate bridging defects with resistances (RBridge) at least up to 3KOhm (see Fig. 8). In that case, in only one of the 1000 runs no one of the three XNOR gates were capable to provide a robust pulse and detect the defect. Note that in this figure at least one of the three XNOR gates generates a robust pulse, as defined earlier, in the 99% of the runs.

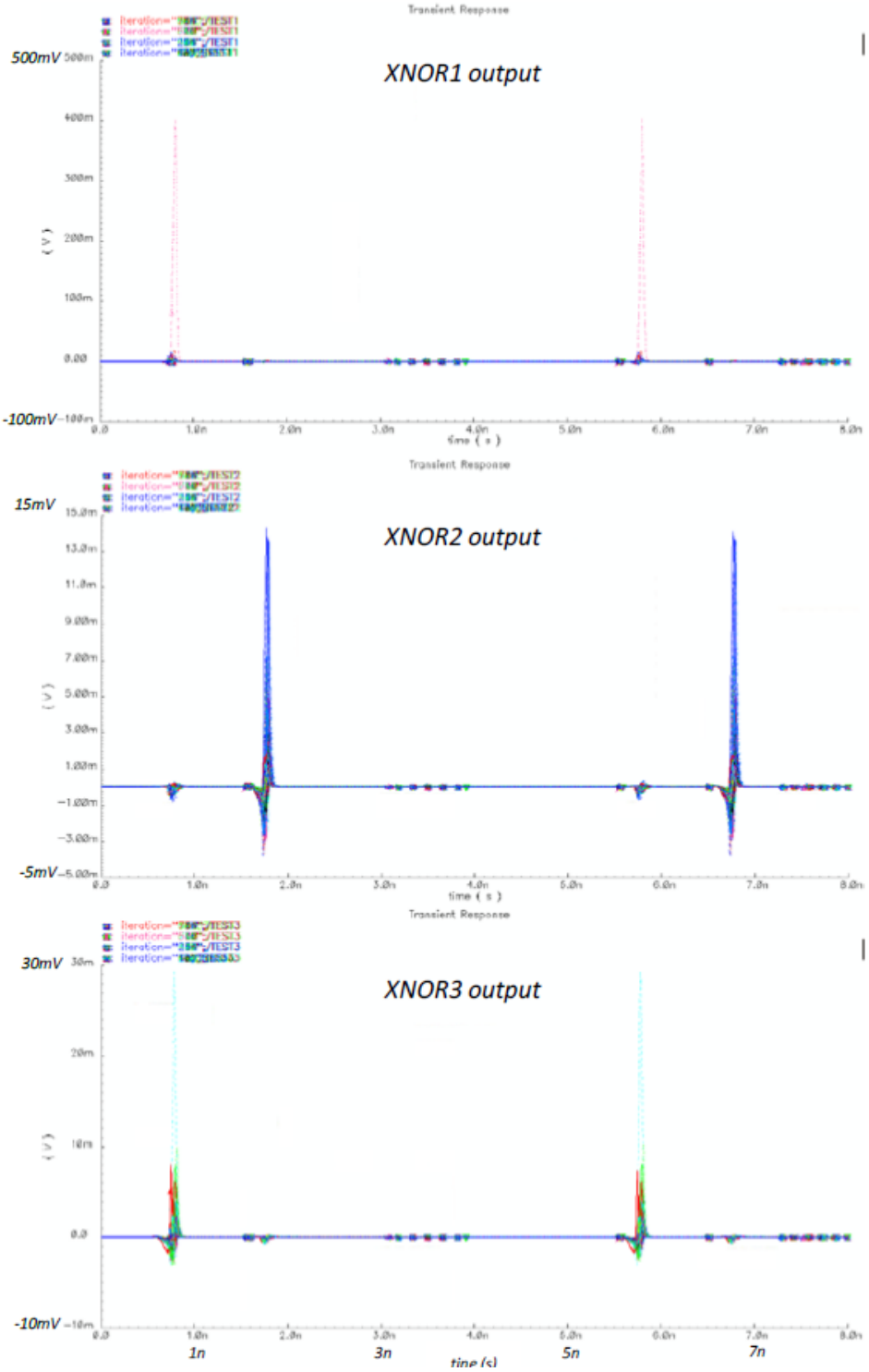

Figure 7: Fault free MC simulation results (1000 runs).

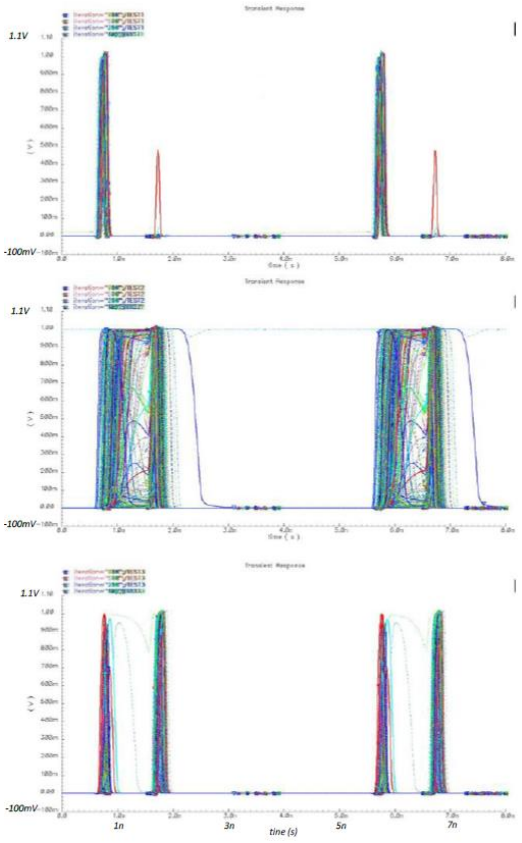

Figure 8: Defective case MC simulation results (1000 runs)

4.3 Comparisons

Table 2 presents qualitative comparisons of the proposed technique with respect to the most recent and advanced technique for testing TSV-to-TSV bridging defects in [11]. The proposed approach is proven to be more efficient over

[11] since:

- it is more effective due to the wider range of detectable bridging defect resistances,
- has lower silicon area cost,
- presents lower design for testability effort due to the all- digital design with the use of standard cells and
- supports the parallel testing of any number of TSVs.

	Proposed Technique	**[11]**
Effectiveness	Detection and location of resistive bridging defects between two TSVs up to **3KOhms** under process and mismatch variations.	Detection and location of resistive bridging defects between two TSVs up to **1KOhm** under process and mismatch variations.
Silicon Area Cost for Testing and Diagnosis	1 MUX, 1 XOR, 1 NOT and 1 Scan Flip-Flop per TSV.	2 MUXs, 2 Flip-Flops, 1 NOT and 3 large size transistors per TSV, plus 1 Analog Comparator.
Design for Testability (DfT) Effort	All-digital design with standard cells.	Analog and digital design with custom and standard cells.
Parallel TSV Testing	Feasible.	Not feasible without the use of a dedicated comparator per TSV or cluster of TSVs.

Table 2. Parameters of the considered TSVs

5. Conclusions

A testing and diagnosis scheme for testing and diagnosis of defective TSVs with respect to resistive TSV-to-TSV bridging defects is proposed. The difference in the delays of two adjacent TSVs that are driven by the complementary signals, is used to detect and locate defective TSVs. An all- digital low-cost, in silicon area and design effort, solution is presented. Monte-Carlo analysis results, which have been conducted using UMC 90nm technology models, shown that this technique is capable to correctly detect defective TSVs for resistance values up to 3KOhms. Comparisons with the most resent and advanced TSV-to-TSV bridging defects testing technique in the literature proved that the proposed testing and diagnosis scheme performs better in terms of effectiveness, robustness, tolerance, cost and design for testability effort. It provides also the ability to test any number of TSVs in parallel.

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