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A Real-Time Edge Accelerator for Coherent Doppler Wind Lidars

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Abstract

The current work presents an Edge Computing hardware accelerator for real-time signal processing in Coherent Doppler Wind Lidars (CDWLs). CDWLs require high-sampling rates that exceed 7 Gbit/s in data throughput for distances above 7.5 km, considering the raw and the accumulated data for noise suppression. The proposed solution exploits a reconfigurable hardware accelerator (Xilinx UltraScale+ MPSoC ZCU102 FPGA) that instantiates 16 parallel processing chains estimating in real-time the wind Doppler shift. The deployed system traces wind speed in 2-digit precision up to 9.99 km range with a spatial resolution of 39.03 m. The hardware accelerator is operating at 245.76 MHz, attaining a processing throughput of 41.94 Gbit/s and utilizing 80210 LUTs, 553 BRAMs and 640 DSPs.

1. Main Text

Coherent Doppler Wind Lidars (CDWLs) provide accurate and high spatial resolution wind speed and direction measurements[1]. The operation principle is as follows: a laser beam is emitted to the atmosphere in pulses via a carrier frequency Fc while the laser's photons interact with the air particles. A small portion of the light reflects to a Lidar receiver as backscattered radiation[2]. Special purpose RF Analog-to-Digital Converters (ADCs) digitize the input signal for further processing. The interaction of the air motion causes a frequency shift to the received signal due to the Doppler effect. As CDWLs broadcast a monochromatic laser of λ wavelength, the wind speed can be estimated by:

$$\vec{u} = \frac{\overrightarrow{\lambda \Delta f}}{2} \quad (1)$$

where $\Delta f f$ is the Doppler frequency shift of the initial carrier frequency. The sign of u⃗ reveals the wind direction: a positive velocity indicates a headwind while a negative indicates a tailwind[3].The majority of CDWLs exploit the Fast Fourier Transform (FFT) analysis to process the received signals in the frequency domain and estimate the Doppler shift ($\Delta f f$). However, interference noise can result in unreliable measurements especially in long-range CDWLs (≥7.5 km) as the SNR decreases proportionally with the range[4]. Respectively, the need for high spatial resolution leads to high sampling rates that increase the raw data volume. Conventional signal processing architectures such as general-purpose CPU-based[5] and Cloud-based processing[6] cannot guarantee real-time operation due to limitations in network bandwidth and storage[7]. Thus, the most efficient solution is to process this data locally in real time, avoiding the

unnecessary data transfers and cold-storage memory usage. This highlights the need for an Edge Computing approach[8]. Special purpose hardware accelerators like Field Programmable Gate Array devices (FPGAs) seems to be suitable for such hard-deadline applications that also provide high-scaling capabilities for processing parallelization[9]. FPGAs also ensure the most efficient Performance-per-Watt FFT implementation, compared to general purpose processors[10]. Thus, while commercial Lidars incorporate Edge Accelerators[11-14] they impose limitations that affect the operational characteristics. Low spatial resolution is a very common issue in long-range CDWLs due to inadequate segmentation of the Line-of-Sight (LoS) distance[12, 14]. Interference noise causes low-accuracy measurements and the proposed noise reduction techniques are too computationally heavy and can adversely affect the real-time operation of CDWLs[11]. Finally, the employed signal processing architectures impose limitations in terms of scalability.

The current work concerns a parallel digital signal processing architecture for real-time signal processing of raw data in long-range CDWLs. It efficiently exploits the available hardware resources in Edge hardware accelerators and provides a scalable solution in Edge Computing wind sensing applications.

2. Related Work

In the literature exists several approaches that applies real-time signal processing techniques to measure wind speed and direction in CDWLs[1]. In work [15], an FPGA-based accelerator for the FFT algorithm is proposed. Although it provides adequate acceleration figures and low latency, the common memory architecture limits the scaling capabilities of the parallel FFT butterfly (compute) units. Unnecessary data transfers between the butterfly units due to the pipeline architecture is also an issue. Similar challenges are present in work [16] where intermediate control registers are employed between the butterfly units. In work [10] the architecture is fully parallel as the pipeline exists only inside each FFT Processing Element (PE), similarly to our implementation: a fully parallel processing architecture based on multiple FFT-based processing chains. The advantage that [10]'s and our approach have is the almost linear scaling with the increasing number of processing elements. Every processing chain features its own dedicated memory to save the processed data. Therefore, additional processing chains can be instantiated, depending on the available hardware resources.

Very few CDWLs are designed for long-range operation. In work [17] a spatial resolution of 1.2 m is obtained. However, the CDWL's measurement range is limited to 1.22 km. It utilizes the Joint-Time Frequency Analysis (JTFA) algorithm as an alternative signal processing method. Although it offers great improvement over using FFT, it is significantly more resource heavy compared and it would be a challenge to implement it in real-time CDWLs. In work [14], the FPGA-based CDWL accelerators consists of 98 spatial segments (gates) with a length of 128 samples, resulting in approximately 77 m spatial resolution over 7.5 km. Even with a CNN model employed to increase measurement accuracy and 16.384 total pulse accumulations, accurate wind velocity measurements cannot be obtained after the 3000 m mark. Another FPGA-based CDWL accelerator is proposed in work [12], the proposed CDWL can obtain measurements over a range of 3.1 km while the spatial resolution is 48 m utilizing 64 gates. This architecture can be extended up to 7 km but will have worse spatial resolution as each gate will need to be longer and as a result require additional ADC samples to provide accurate measurements. In work [11], the proposed real-time long-range FPGA CDWL accelerator employs 500 gates in the maximum-area configuration. However, the presented measurement results indicate very poor accuracy above 5

km indicating limitations in the implemented signal processing subsystem. Our proposed accelerator is instantiated in a Xilinx UltraScale+ MPSoC ZCU102 FPGA & features 16 parallel processing chains while each utilizes a Xilinx FFT LogiCORE IP core configured at N_{FFT}=1024. A spatial resolution of 39.03 m is achieved by utilizing 256 gates for a maximum detection range of 9.99 km. The generated 7.68 Gbit/s of raw input data are processed in real-time and the total processing throughput (when also considering the accumulated redundant data) is approximately 41.94 Gbit/s. Absolute wind velocity error of less than 0.075 m/s is attained by exploiting the MCA method. Data transfers are minimized as each processing chain features a dedicated memory while a full accumulation takes less than 3 ms, enabling real-time operation. Concluding, we used more gates than most previous works while also performing many accumulations to obtain accurate measurements.

3. System Architecture

The system architecture of a Coherent Doppler Wind Lidar is presented in Fig. 1.

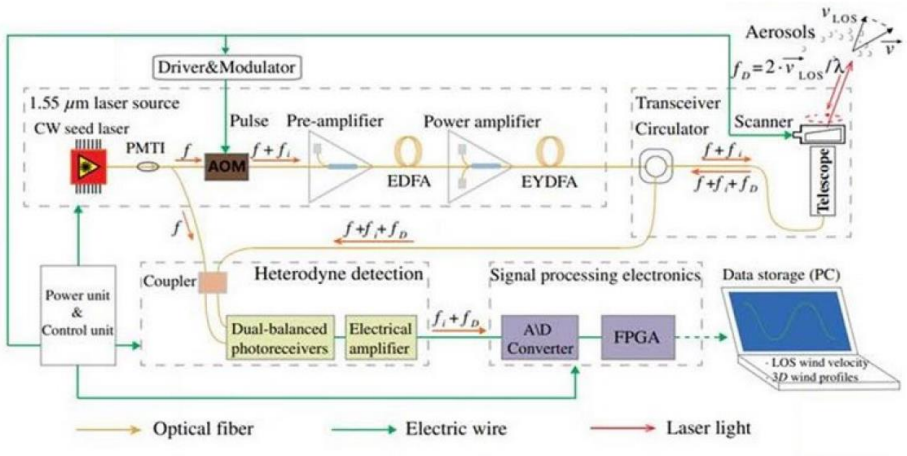

Figure 1: System architecture

A seed source generates a CW laser light. An optical splitter is used to separate the laser beam in two segments: one towards the transmitter and the other into a local oscillator. The first beam passes through an Acoustic-Optical Modulator (AOM) which down-converts it to the RF spectrum in two sequential pulses of carrier frequency Fc . The pulse repetition frequency Fpul is an external square wave pulse that is fed to the AOM and defines the Wind Lidar measurement cycle. The beam is amplified as it passes through an optical amplifier called Erbium-Doped Fiber Amplifier (EDFA). Next, the amplified pulse goes through a passive circulator and is emitted to the atmosphere via the telescope. The telescope is also responsible for the collection of the backscattered radiation during the scan phase. The collected radiation then goes through the mixer alongside the second beam of the local oscillator and goes into the Detector Unit. The Detector is a hybrid unit as it contains a non-directional coupler (to split internally split the input signal) as well as two directional couplers to produce an IQ (In-Phase & Quadrature) response, resulting in two outputs that are 90 degrees out of phase. Then, these two RF signals are connected to the inputs of a dual Analog-to-Digital Converter (ADC). Finally, the quantized information is fed to the DSP hardware accelerator which is inferred in an SoC FPGA.

3.1 Analog Subsystem

The major building component of CDWLs is the Continuous Wave (CW) laser seed. The CW laser should have adequate power as it will have to withstand distortion caused by multiple noise sources. State-of-the-art Coherent Lidars use infrared light for better performance [1, 18]. The Acoustic-Optical Modulator (AOM) shifts the inputs from the Optical Frequency range to the Radio Frequency (RF) range. The employed AOM makes the signal "pulsed" as the previously continuous signal now has a fixed repetition period. It is a necessary component of every Coherent Lidar as Coherent reception cannot be implemented using CW laser. The telescope is responsible for interacting with the environment by transmitting and receiving radiation. The receiver is embedded in the telescope, and it is responsible for converting the optical backscattered radiation to electrical RF signals. It is based on a hybrid detector, as it features an internal directional coupler to split the input in two 90 degrees out-of-phase signals: In-phase (I) and Quadrature (Q).

3.2 Digital Subsystem

The ADC is responsible for quantizing the Heterodyne Detector's responses (I & Q). The ADC produces samples with nn-bits of precision, meaning that nn−1 bits succeed the decimal point. The FPGA receives samples from the ADC at a constant rate and embodies a parallel FFT chain-based signal processing architecture. It also provides the necessary memory resources to save all the partial processing steps until all the computations are performed.

The Lidar's pulse repetition frequency (Fpul) defines the time delta in which the Lidar will be receiving the detected backscattered pulses. It also defines the Lidar's maximum LoS detection radius RDmax=2/cFpul, where c is the speed of light in the atmosphere. The maximum Lidar range is half of the distance the light travels in ΔT=1/Fpul time as the light needs to cover 2d distance to measure wind over a distance d. As shown in Fig. 2, the Spatial Resolution (SR) is equal to the gate length as the LoS radius is segmented in Np gates of equal length[19]:

$$SR = G_l = \frac{R_D}{N_p} \quad (2)$$

The corresponding gate length in samples (Lg) depends on the ADC's sampling rate (Fs), pulse repetition frequency (Fpul), the total number of gates ($NNpp$) and the ratio k=RD/RDmax as follows: Lg=kFs/FpulNp. The signal processing architecture and the spatial segmentation will be discussed in detail in section 5.

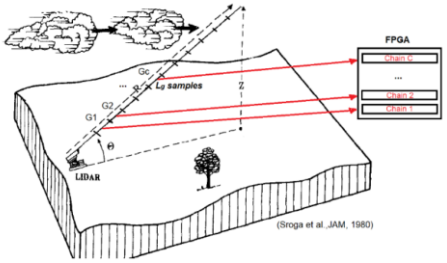

Figure 2: Geometry of CDWL gates [19]

4. Noise Modeling

The main challenge in the operation of CDWL is the interference noise effects. Several sources of electromagnetic radiation exist in the environment such as solar radiation, telecommunication antennas and infrared radiation which is emit by heated objects. Additionally, optical and

electrical components introduce noise, such as the receiver's Avalanche Photodiode (APD) and the pre-amplifier. To obtain useful information from the received backscattered radiation we first must analyze the nature of the noise, the perceived SNR and then we must implement the appropriate denoising technique for the target CDWL application.

In coherent Lidars[20], the SNR is expressed as:

$$\mathrm{SNR_{CL}} = \frac{\mathrm{P_R m \eta_m}}{\eta \nu \mathrm{B}} \quad (3)$$

where $PPRR$ is the average input power at the Lidar receiver, mm is the heterodyne mixing efficiency, ηmm is the mixer quantum efficiency, hν is the photon energy and BB the receiver noise bandwidth.

A more generic approach to measure SNR is to consider the peak power SNR[18]:

$$\mathrm{SNR} = 20\log\left(\frac{A_p}{\bar{u}}\right) \quad (4)$$

where $AApp$ is the input signal RMS power at the Lidar receiver and uu⍰ the RMS power of the noise. The noise can be further analyzed as:

$$\bar{u} = \sqrt{\overline{u_{APD}^2} + \overline{u_B^2} + \overline{u_{Pa}^2}} \quad (5)$$

where $\overline{u_{APD}}$ is the Lidar detector noise, $\overline{u_B}$ is the background noise and $\overline{u_{Pa}}$ is the pre-amplifier noise. From these three noise components, the most important is the background noise $\overline{u_B}$. Because the background noise is essentially the signal distortion as the emitted light travels in the atmosphere, coherently detected signals can be modeled as narrowband RF signals with additive white Gaussian noise (AWGN). Although filtering AWGN is near impossible as it affects the whole frequency spectrum, we can eliminate it knowing that the backscattered radiation is concentrated close to F_c. The most common way to suppress AWGN in CDWLs is to accumulate multiple pulse responses, a method also known as Multi-Pulse Coherent Accumulation (MCA)[18]. For each sampled pulse per gate, the frequency response is measured and the corresponding power spectrum is derived. These spectra are then accumulated for a defined number of accumulations PP. This will greatly reduce the complexity of the design (as now only positive values will have to be handled). After PP accumulations, we determine the dominant frequency and from there we calculate the wind speed and direction. The effective SNR using the MCA method is as follows:

$$SNR_{MCA} = 20log\sqrt{P} + SNR_0 \quad (6)$$

The minimum required number of accumulations to reliably calculate the Doppler shift (P_{min}) is based on the accumulated SNR_{MCA} and is as follows:

$$\overline{f_{error}} = |f_{dpul} - \overline{f_d}| \quad (7)$$

where

$$\overline{f_d} = \frac{\Sigma_{1_{i=1}^{P}}(f_d)i}{P} \quad (8)$$

Σ1i=1Pminrepresents the accumulated pulses, f_{dpul} the actual frequency of the backscattered pulse and $ffdd$ the detected pulse frequency. To minimize f_{error}, a MATLAB model to estimate the minimum number of accumulations needed in relation to the noise power was developed. The

absolute error of the FFT was set to $f_{error} \leq 0.1$ MHz. Our model features the following input parameters: the SNR of the output signal after the introduction of AWGN, the F_{var} and I_{var} parameters which define the distortion variation of the initial pulse wave in frequency and amplitude respectively and Lg. The model performs multiple regressions until the target of 0.1 MHz is achieved and then returns the P_{min} value. The model reveals the relationship between Lg and computation accuracy.

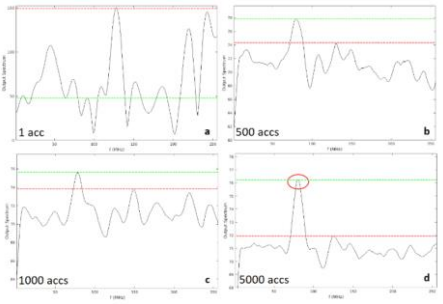

Figure 3: Average power spectrum after 1, 500, 1000 & 5000 accumulations

The analysis of a single noisy input frame of L_g samples leads to a totally unreliable determination of the signal's main frequency (Fig. 3a). By repeating the analysis up to a total of P times, in each iteration a new frame will provide a different, randomly varied response from the emitted signal which will be accumulated to form the final spectrum (Fig. 3a-3c). The simulation results for various configurations after a series of simulations are presented in Table 1. The three-way correlation between L_g, total accumulations and noise is presented in Fig. 4.

AWGN		**-10 dB**		**-20dB**
(Ivar , Fvar)	(0.2, 0.2)	(0.5, 1)	(0.2, 0.2)	(0.5, 1)
Lg = 32	2630 accs	3010 accs	9550 accs	15620 accs
Lg = 64	330 accs	620 accs	3900 accs	6020 accs

Table 1 Minimum accumulations for error ≤0.1 MHz

5. Real-Time Signal Processing Architecture

5.1 Processing Chain

The major challenge in real-time Lidar applications is to extract information from very high amount of data. The FFT analysis is employed to obtain the frequency content. Based on the shift from the initial frequency (Fc) the wind speed and direction will be measured for that specific time frame.

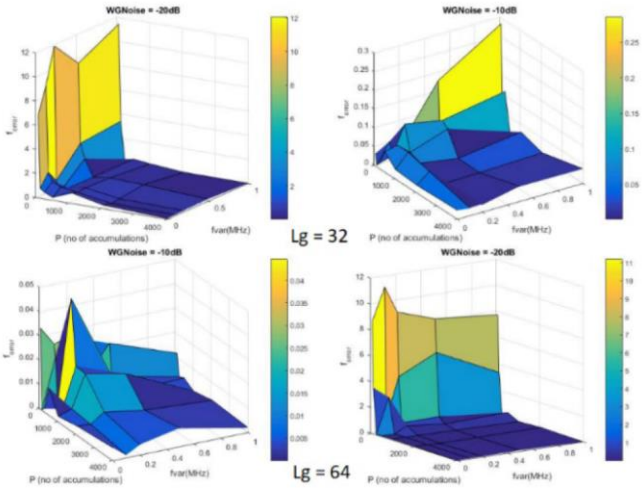

Figure 4: Detected frequency error scaling

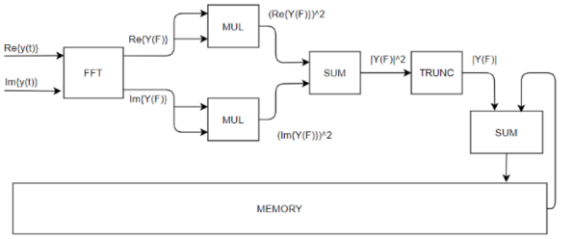

Figure 5: Architecture of FFT processing chain

The processing chain architecture is shown in Fig. 5. This consists of an FFT IP core to generate the frequency response of the two inputs from the ADC (I & Q). The FFT produces the spectrum in two signals (I & Q). Next, two multiplier modules are utilized to calculate the power of 2 (square) output of each input. The output of each multiplier is then summed using a Full Adder (FA) module. The output of the FA will then be truncated using the TRUNC block instead of a resource-heavy square root block. The final calculated power spectrum from this step is then saved to the block memory of the FPGA.

To optimize accuracy and avoid very long FFT lengths, the parabola fitting estimator is employed. Instead of depending only on the dominant FFT point, the 2 neighboring ones are also considered as follows:

$$P_{max} = \frac{P_a - Pc}{2(Pa - 2Pb + Pc)} \quad (9)$$

where: P_{max} is the offset to be added to maxpos (index of the dominant FFT point), P_b is the value of the spectrum of the dominant FFT point, P_a is the value of the spectrum for the FFT point at position -1 from the dominant, P_c the value of the spectrum for the FFT point at position +1 from the dominant and therefore max_p=maxpos+P_{max}. Finally, we multiply max_p with the precision N_p of the FFT and the final frequency is obtained as f=$max_p N_p$.

5.2 Chain Parallelism

The wind Lidar's radius (R_D) is segmented in N_p=R_D/G_l (spatial) gates where GGl is the physical gate length. A single processing chain is employed for the measurements of C_g=N_p/C gates. The

window size (W_s=N_pL_g) represents the total number of samples per measurement cycle across all gates. In Fig. 6 the sample distribution to the C parallel processing chains is shown. In every new measurement, the first L_g samples are directed to chain No.1. The next L_g samples are directed to chain No.2 and so on. After chain No. C is successfully fed with data, the next L_g samples are directed to chain No.1 and the cycle starts over. Special care must be taken regarding the processing timing as the first chain must have fully completed the previous operation before it receives new pulse data. It is apparent that more parallel processing chains enable data processing for CDWLs with higher gate counts. Additionally, each FFT compute unit receives N_p non-zero values and N_{FFT}–N_p zero-values. This technique is known as "zero-padding" and contributes to better spatial resolution.

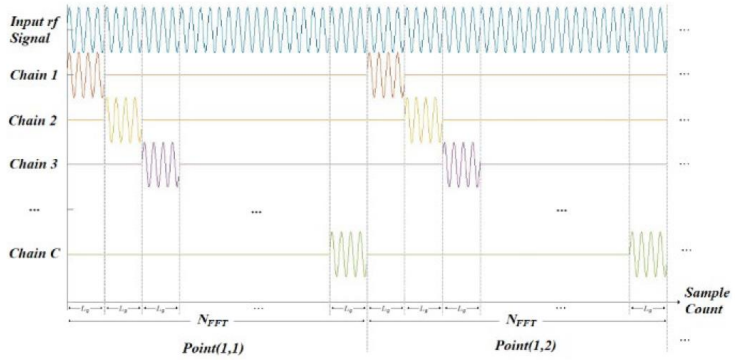

Figure 6: Parallel processing chains & sample distribution

The gate distribution depends on the available hardware resources. The advantage of inferring more parallel chains is more relaxed timing constraints as each chain will have more time to complete a full accumulation. The maximum execution latency is as follows:

$$t_{ex\_max} = C_g L_g \frac{1}{F_{pul}} \tag{10}$$

More parallel processing chains alongside more samples per gate will result in higher execution latencies which are easier to attain. For example, 256 gates can be split as 8, 16 or 32 parallel processing chains, each processing samples for 32, 16 or 8 gates respectively. An arbiter unit is employed to direct the samples in from the ADC to the parallel processing chains in frames of L_g samples. Enough time should be allowed for each FFT to process the input samples. After C frames all the FFT units will have received samples at least once.

As the arbiter continues to feed with data the parallel processing chains, after some time we will have gone through all the N_p gates. This process continues and the new spectra are accumulated to the previous ones. After PP accumulations, a mean spectrum is derived for each of the N_p.

6. Experimental Results

The schematic of FPGA implementation of our proposed parallel CDWL signal processing architecture is presented in Fig. 7. Specifically, the CDWL processing architecture is configured as follows: Fs = 245.76 MSPS, Fpul = 10 KHz, k = 0.66, Np = 256, NFFT= 1024 and PP = 10000 accumulations. This resulted in the following CDWL properties: RD = 9.99 km, Ws= 16384, Lg=64 and Gl = 39.03 m.

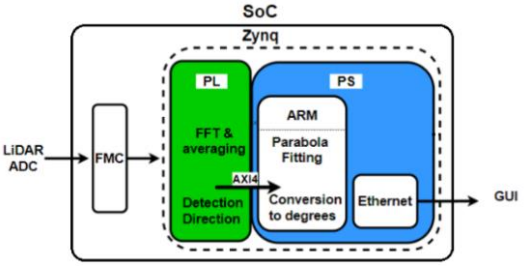

Figure 7: Proposed CDWL architecture

The analog compartment of the CDWL consists of a 1550nm λ CW laser seed and an AOM with a central frequency of Fc = 80 MHz which indicates the zero Doppler shift of the emitted pulse. The ADC generates the corresponding samples of our two inputs (I & Q) and each sample consists of 16-bits. The 256 gates are distributed in 16 parallel processing chains. As a result, a total of 16 spectra are stored & accumulated in each processing chain. Each spectrum consists of 1024 32-bit samples to fully exploit the FPGA's RAM block architecture. Based on that, 16 RAM blocks are inferred in each processing chain to store the 16 distinct spectra.

6.1 Resource Utilization & Timing

The resource utilization (Table 2) indicates heavy BRAM usage (over 60%) due to the dedicated memory of each processing chain while for the rest FPGA resources, we observe a more moderate utilization up to 30%. Total Execution Time depends solely on the pulse repetition frequency Fpul and the total number of accumulations P as follows: t_totalex=P/Fpul. From Eq.10, the maximum accumulation latency is estimated at 4166 ns. The actual latency induced by the processing chains for each accumulation is 2918 ns considering the critical path. Total input data rate equals 7.86 Gbit/s while the processing throughput (when also considering the accumulated redundant data) is 163.84 Mbit/s per processing chain. Therefore, the total processing throughput of our accelerator considering the 16 parallel processing chains is 41.94 Gbit/s. The (theoretical) minimum total execution time is 41.66 ms considering P = 10000 accumulations, zero-wait sample arrival, no sample dropping and maximum pulse repetition frequency (Fpul = 240 KHz). We also experimented with more than 256 gates. Indicatively, an architecture with 64 parallel chains was synthesized. As expected, the scaling was almost linear and therefore the design couldn't fit to our FPGA requiring 240% BRAM. However, the in-chain execution latency was not affected by this change which shows that our proposed parallel architecture is indeed scalable. For reference, a design using the previous configuration (64 processing chains, 16 gates per chain) and a sampling rate of Fs = 983.04 MSPS while keeping the system's clock frequency at 245.76 MHz would result in quadruplication of the total processing throughput, exceeding 167 Gbit/s.

	LUT	LUTRAM	DFF	DSP	BRAM	Clock Frequency (MHz)
Util.	80210	13347	117515	640	553	245.76
Util. %	29.27	9.27	21.24	25.40	60.64	

Table 2 FPGA resource utilization

6.2 Results & Design Verification

The simulated spectral accumulation in Xilinx Vivado for a single processing chain is shown in Fig. 8. In each consecutive accumulation, the chain receives new data from the FFT and the average power trends upwards (as indicated by the "step" form of the waveform in Fig. 8).

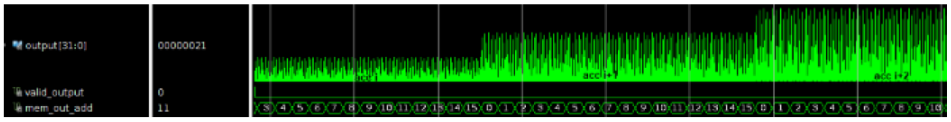

Figure 8: Spectral accumulation

After 10.000 accumulations, we perform a close-up inspection of a single gate (Fig. 9) to determine if -based on the input data- the detected frequency is the expected one while also considering the Parabola Fit estimator. The analysis shown that the maximum absolute frequency error was at most 0.093 MHz. This shows that our previous estimation of ≤0.1 MHz error was valid and the processing chain performs as expected. We also note that no timing violations were reported by Vivado, and therefore the correct functionality is assured.

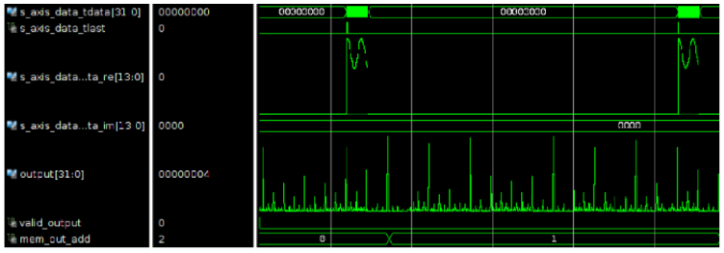

Figure 9: Single gate spectrum

7. Conclusion

In this paper, we propose a real-time signal processing hardware accelerator for CDWLs at the Edge. Wind measurements for 256 spatial gates over 9.99 km LoS range and a spatial resolution of 39.03 m are realized. A Xilinx FPGA hosts 16 parallel processing chains, each responsible for processing samples for 16 gates. By performing 10.000 MCA accumulations, the absolute wind velocity error is capped at ≤0.075 m/s. The computation-heavy parts of the CDWL architecture (FFT and spectral accumulations) are performed entirely on the FPGA and unnecessary data transfers are avoided. Finally, our architecture provides high processing throughput of 41.94 Gbits/s while it is offers great scalability due to the inherent parallelism of the processing chains.

References

[1] C. Werner, “Doppler Wind Lidar,” Lidar: Range-Resolved Optical Remote Sensing of the Atmosphere, vol. 102, pp. 325, 2006.

[2] F. Chouza, O. Reitebuch, and Gro, “Retrieval of aerosol backscatter and extinction from airborne coherent Doppler wind lidar measurements,” Atmospheric Measurement Techniques, vol. 8, no. 7, pp. 2909--2926, 2015.

[3] M. I. Skolnik, "36 - Radar," Reference Data for Engineers (Ninth Edition), M. M. Wendy and E. Mac, eds., pp. 36-1-36-22, Woburn: Newnes, 2002.

[4] N. Berger, “Understanding and Utilizing Power Density,” Laser Surgery in Veterinary Medicine, pp. 14--21, 2019.

[5] F. H. Khan, M. A. Pasha, and S. Masud, “Advancements in microprocessor architecture for ubiquitous AI—An overview on history, evolution, and upcoming challenges in AI implementation,” Micromachines, vol. 12, no. 6, pp. 665, 2021.
[6] A. Sunyaev, "Cloud computing," Internet computing, pp. 195--236, 2020.
[7] M. Kumar, K. Dubey, and R. Pandey, “Evolution of emerging computing paradigm cloud to fog: applications, limitations and research challenges,” 2021, pp. 257--261.
[8] W. Shi, J. Cao, Q. Zhang, Y. Li, and L. Xu, “Edge computing: Vision and challenges,” IEEE internet of things journal, vol. 3, no. 5, pp. 637--646, 2016.
[9] C. Xu, S. Jiang, G. Luo, G. Sun, N. An, G. Huang, and X. Liu, “The case for FPGA-based edge computing,” IEEE Transactions on Mobile Computing, 2020.
[10] I. S. Uzun, A. Amira, and A. Bouridane, “FPGA implementations of fast Fourier transforms for real-time signal and image processing,” IEE Proceedings-Vision, Image and Signal Processing, vol. 152, no. 3, pp. 283--296, 2005.
[11] Vasiljevi, “Long-range WindScanner system,” Remote Sensing, vol. 8, no. 11, pp. 896, 2016.
[12] S. Abdelazim, D. Santoro, M. F. Arend, F. Moshary, and S. Ahmed, "Coherent Doppler Lidar for wind sensing," Spatial Variability in Environmental Science-Patterns, Processes, and Analyses, 2020.
[13] O. Kliebisch, and P. Mahnke, “Real-time laser Doppler anemometry for optical air data applications in low aerosol environments,” Review of Scientific Instruments, vol. 91, no. 9, pp. 095106, 2020.
[14] O. Kliebisch, H. Uittenbosch, J. Thurn, and P. Mahnke, “Coherent Doppler wind lidar with real-time wind processing and low signal-to-noise ratio reconstruction based on a convolutional neural network,” Optics Express, vol. 30, no. 4, pp. 5540--5552, 2022.
[15] J. Chen, Y. Lei, Y. Peng, T. He, and Z. Deng, “Configurable Floating-Point FFT Accelerator on FPGA Based Multiple-Rotation CORDIC,” Chinese Journal of Electronics, vol. 25, no. 6, pp. 1063--1070, 2016.
[16] B. Zhou, Y. Peng, and D. Hwang, “Pipeline FFT architectures optimized for FPGAs,” International Journal of Reconfigurable Computing, vol. 2009, 2009.
[17] C. Wang, H. Xia, Y. Liu, S. Lin, X. Dou, and R. M. Hardesty, “Spatial resolution enhancement of coherent Doppler wind lidar using joint time-frequency analysis Performance of a discrete spectral peak frequency estimator for Doppler wind velocity measurements,” Optics Communications, vol. 424, no. 5, pp. 48--53, 2018.
[18] X. Li, and P. Luo, “Boosting ranging performance of LiDAR using multi-pulse coherent average,” IEEE Sensors Journal, vol. 19, no. 15, pp. 6270--6278, 2019.
[19] J. T. Sroga, E. W. Eloranta, and T. Barber, “Lidar measurement of wind velocity profiles in the boundary layer,” Journal of Applied Meteorology and Climatology, vol. 19, no. 5, pp. 598--605, 1980.
[20] W. R. Leeb, P. J. Winzer, and K. H. Kudielka, “Aperture dependence of the mixing efficiency, the signal-to-noise ratio, and the speckle number in coherent lidar receivers,” Applied optics, vol. 37, no. 15, pp. 3143--3148, 1998.
[21] G.-E. Liatsos, “Digital processing system for Coherent Detection Wind LiDAR with SoC FPGA,” 2020.