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Fractional-N Phase Locked Loop for Wi-Fi 6/6E With 135 mW Power Consumption and Spur Reduction Techniques

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Abstract

This paper presents a fractional-N phase locked loop (PLL) for Wi-Fi 6/6E applications in 28 nm FD-SOI CMOS technology. The PLL consists of an LC voltage-controlled oscillator (VCO), a dual edge phase-frequency detector (PFD), a programmable charge pump with linearization scheme, a prescaler, a fully integrated low pass filter and a 3rd order Sigma-Delta modulator to control a programmable divider. Notable features include fast automatic frequency locking, and optimal loop bandwidth (LBW) and VCO amplitude calibration. The PLL draws current from a 1.8 V supply, having a power consumption of 135 mW. The reference clock is 60 MHz, RMS jitter is 161.9 fs (1 kHz – 100 MHz) and the reference spur level is -55 dBc.

1 Introduction

Phase-Locked Loops (PLLs) (Razavi, 2020) play a crucial role in modern wireless communications. The PLL is one of the key building blocks of RF front-end transceivers, generating the local oscillator (LO) signal. The LO signal specifications, i.e. phase noise and frequency, are determined by the wireless standard. The PLL presented in this paper targets Wi-Fi 6/6E standard specifications. Key performance metrics of a PLL include strong suppression of reference and harmonic spurs, low RMS jitter and minimal power consumption. This work presents a fractional PLL with output frequency range 6.5 – 9.7 GHz.

2 System Architecture

The proposed fractional-N PLL generates the LO clocks for the wireless transceiver. Figure 1 shows the block diagram of the Fractional-N frequency synthesizer architecture. Charge-pump based topology is selected to achieve high-end phase noise performance. Multiple oscillator cores ensure VCO noise optimization over frequency in the expense of additional area. To suppress reference spur and Sigma-Delta modulator noise, a 4th order, programmable low pass filter has been implemented. The optimum loop bandwidth for the specific design is around 500 kHz. Digital logic controls the PLL parameters so that it operates as close as possible to the optimum bandwidth and achieves fast lock time. The lock time including calibration is less than 50 μs. Fast lock time is required to enable fast channel hopping in certain wireless protocols such as Bluetooth Low Energy. Special techniques to compensate for the dynamic phase error introduced by the Sigma-Delta modulator, which elevates fractional spur power levels, have been deployed.

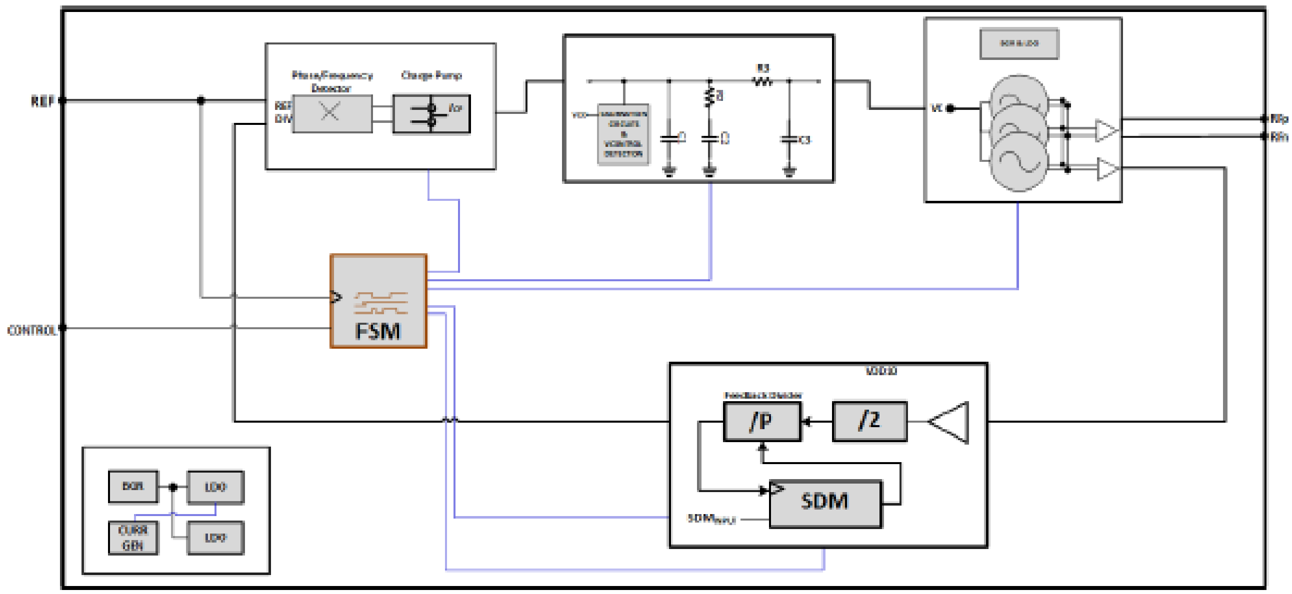

Figure 1: PLL block diagram

2.1. PFD & Charge Pump

The phase frequency detector (PFD) and the charge pump (CP) are used to convert the phase difference between the reference and the feedback signals to a proportional current signal. An important PFD operation is to "recognize" which pulse is leading or lagging, causing the charge pump to either sink or source current. The PFD can detect the phase difference of both positive and negative edges of the reference and feedback signals, effectively doubling the reference signal frequency. Using a clock doubler instead would increase the phase noise by 6 dB, since the phase noise of the multiplied signal increases with the multiplication factor.

When designing the PFD and CP, the main targets are to minimize spurious frequencies, phase noise and power consumption. Common factors that can increase the spurious tones are the dead zone of the PFD, and CP current mismatches and off-state leakage. Isolating the CP current mirrors from the local bias using sample & hold scheme results in reduced output noise. Special attention has been paid to fractional spur suppression. Dedicated circuits are used to force the CP to operate in a linear region and to compensate for the instantaneous phase error introduced by the Sigma-Delta modulator. As shown in Figure 2 (b), to reduce current mismatch, the bias current $\mathrm{I_{bias}}$ is generated by a bandgap reference and the operational amplifier, used as a buffer, forces $\mathrm{CP_{out}}$ and the other branch to have the same voltage. The top left operational amplifier regulates the PMOS current mirror gate voltage, while $\mathrm{CP_{out}}$ is fluctuating.

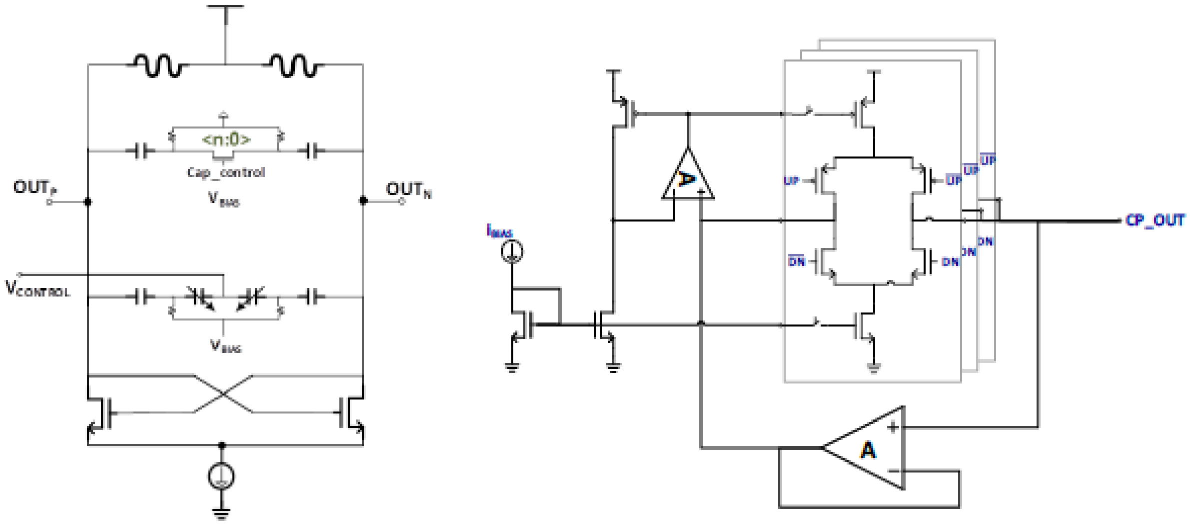

Figure 2: (a) VCO architecture, **(b)** Charge Pump

2.2. VCO

Figure 2 (a) shows the VCO architecture, which has a frequency range from 6.5 GHz to 9.7 GHz. To cover this frequency range, the VCO consists of three cores. Each core utilizes a custom 8-shaped, high Q inductor, which is the best shape to minimize the effect of PA pulling. The architecture employs digitally controlled binary and thermometer-coded capacitor banks controlled by digital logic to allow tuning of the VCO to the desired frequencies over process, voltage, and temperature (PVT) variations. The capacitor banks are designed to achieve more than 60% frequency overlap between the bands over PVT variations and mismatch. Also, a network of varactors is employed to realize fine frequency tuning with a gain that ranges between 35 MHz/V and 120 MHz/V over PVT variations and frequency bands. High level layout EM extracted views have been used in the simulations, resulting in excellent correlation of the simulation results with the lab measurements.

2.3. Sigma-Delta Modulator

The digital Sigma-Delta modulator (SDM) is used to modify the division ratio of the PLL feedback divider to achieve fractional division. A 3rd order modulator has been implemented so that there is minimal impact on the PLL phase noise due to the SDM quantization noise. The SDM design uses a single stage multiple feedback topology to avoid the frequency spurs that are present in the output spectrum of typical MASH 1-1-1 SDM. Furthermore, the output range of the SDM used in the presented PLL can be decreased to reduce PLL near-in frequency spurs due to charge pump non-linearity.

2.4. Digital calibration logic

Digital calibration logic has been implemented to boost PLL performance and automate PLL configuration to allow for faster lock time. The digital calibration finite state machine (FSM) performs four kinds of calibration: VCO frequency tuning, VCO amplitude, PLL loop bandwidth, and VCO core selection.

VCO frequency tuning calibration is used to find the VCO capacitor bank configuration that results in an open loop VCO output frequency as close as possible to the target one for a given VCO varactor control voltage. To achieve the highest possible margin due to temperature variations, the VCO varactor control voltage during VCO frequency tuning calibration should be equal to the middle value of the varactor control voltage range.

VCO amplitude calibration is used to target a specific VCO amplitude that minimizes VCO phase noise. Due to PVT variations the VCO current that results in a specific VCO output amplitude is not constant. The calibration logic utilizes the VCO amplitude detector to set the VCO output amplitude to the target value. Since VCO output amplitude is affected by the VCO frequency, VCO amplitude calibration is performed in tandem with VCO frequency tuning calibration.

PLL loop bandwidth calibration is used to set the PLL loop bandwidth to a certain target value that minimizes phase noise when the PLL is locked. It is possible to control the PLL loop bandwidth by modifying the closed loop gain, which depends on the VCO frequency gain (MHz/V), the feedback signal gain, the PFD/CP gain, and the low-pass filter gain. For a given PLL output frequency only the low-pass filter and the PFD/CP gains can be modified since all other gains cannot be directly controlled. However, to accurately set the PLL loop bandwidth all the gain values must be known. The feedback signal gain is dictated by the feedback path division ratio and therefore it is known. The PFD/CP and low-pass filter gains are controlled by PLL loop bandwidth calibration, so their values are also known. VCO frequency gain depends on PVT variations and therefore it must be measured by the digital calibration FSM. Once the VCO frequency gain is known, all the different gain values are combined to set the CP current and the PLL low-pass filter resistance to the values that result in the target PLL loop bandwidth.

Due to PVT variations some PLL output frequencies, near the boundaries of the VCO core frequency ranges, can be generated by different VCO cores. Therefore, we cannot always assign the same VCO core for a given PLL output frequency. VCO core selection calibration is used to automatically select the VCO core for a specific PLL output frequency.

3 Modeling and Measurements

PLL low pass filter design, and optimum CP current and VCO gain selections were based on a PLL system model developed in Matlab. The system model utilizes all the PLL sub-block noise transfer functions and noise specifications to calculate the PLL output phase noise contribution of each PLL sub-block as shown in Figure 3.

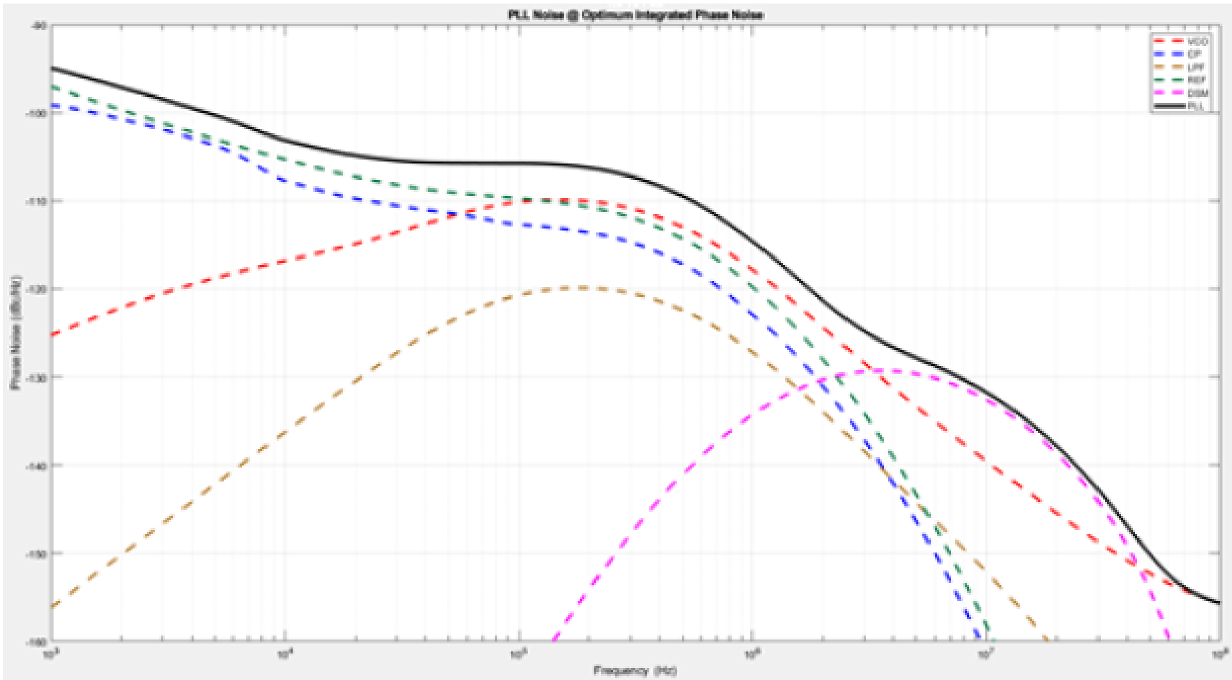

Figure 3: PLL phase noise contributions calculated using the system model

The PLL measurements were conducted through the transmitter chain output, meaning that the Tx LO signal is measured rather than the actual PLL output. The phase noise measurements at 5.18 GHz and at 7.12 GHz are depicted in Figure 44 (a) and (c) respectively. Please note that there are no visible in-band spurs (Figure 4 (b)). The reference spurs are 55 dB lower than the carrier, which is extremely low given the low reference signal frequency. Finally, in Figure 4 (d) the PLL layout is shown.

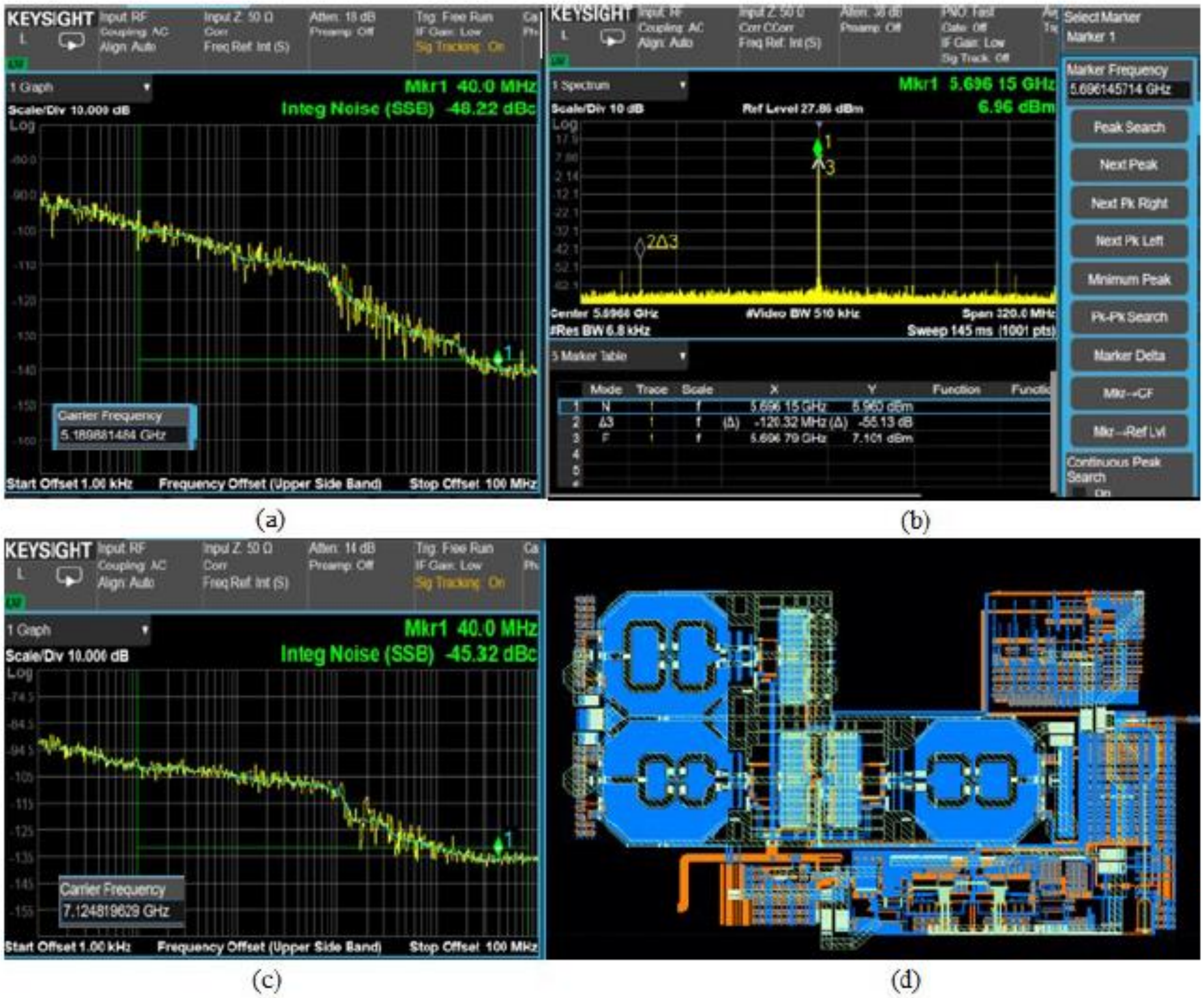

Figure 4: (a) Phase noise measured at @5.18 GHz, **(b)** Reference spur level @5.06 GHz **(c)** Phase noise measured @7.12 GHz, **(d)** PLL layout

4 Conclusions

In this paper, a PLL with output frequency range 6.5 – 9.7 GHz and many different spur reduction techniques has been presented. Furthermore, digital logic has been implemented to enable loop bandwidth calibration, fast automatic frequency locking, automatic VCO core selection and VCO amplitude calibration.

The comparison of our PLL with other state-of-the-art PLLs for Wi-Fi applications is shown in Table 1. To facilitate comparison, phase noise performance of all PLLs has been normalized to 1 GHz using the formula $PN_{norm} = PN - 20\log\left({}^{F_{out}}/_{1\ GHz}\right)$. Since the PLLs we compare to use different reference signal frequencies, we cannot directly compare phase noise performance. A well-known figure of merit (FoM) that takes into account RMS jitter, power consumption and the reference signal frequency (Bae, 2022) is:

$$FOM_{JR} = 10\log\left[\left(\frac{\sigma_{rms}}{1s}\right)^2 \left(\frac{P_{pLL}}{1\ mW}\right) \left(\frac{f_{ref}}{1\ MHz}\right)^{1.5}\right]$$

where σ_{rms} is the PLL RMS jitter, $P_{pLL}$is the PLL power consumption and f_{ref} is the PLL reference signal frequency. As it can be seen in Table 1 the FoM of the presented PLL achieves the same or better performance than other works.

	(Didem Turker, 2018)	(Mayank Raj, 2017)	(Yue-Fang Kuo, 2022)	**This work @7.12 GHz**
Technology	16 nm FinFET	16 nm FinFET	TSMC 180 nm	**28 nm FD-SOI**
Number of LC VCO(s)	2	2	1	**3**
Reference freq. [MHz]	500	450	198.6 – 216.3	**60**
Frequency range [GHz]	7.4 – 14.0	9.0 – 18.0	6.42 – 6.92	**6.5 – 9.7**
Phase noise @100 kHz	-135.9	-129.2	N.A.	**-122**
Phase noise @1 MHz	-139.1	-132.4	-132	**-137**
RMS jitter [fs]	53.6	164	N.A.	**161.9**
Reference spur [dBc]	-75.5	N.A.	N.A.	**-55**
Power [mW]	45	29.2	3.1	**135**
Area [mm^2]	0.35	0.39	N.A.	**1.66**
FoM_{JR}	-148.4	-141.3	N.A.	**-147.9**

Table 1: Performance summary and comparison

The proposed PLL exhibits phase noise performance that can support the highest data rate (MCS-11) for Wi-Fi 6/6E applications, while using a low frequency reference signal. Furthermore, the low reference spur power level minimizes interference from neighboring channels. Finally, due to the digital calibration logic employed in this PLL the lock time is less than 50 µs, allowing its usage in applications that require fast frequency hopping, such as Bluetooth Low Energy.

5 References

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