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Development and validation of the AcubeSAT nanosatellite communications module

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**Abstract**

AcubeSAT is an open-source nanosatellite project which will study the effects of micro gravity and radiation on microorganism cells. Its communication needs are served by the SatNOGS COMMS Board, a board initially designed by Libre Space Foundation (LSF) and modified accordingly by SpaceDot for its mission requirements. In this paper, we provide an overview of the functionality of the board, the in-house software and FPGA development as well as a detailed presentation of the board's testing and validation procedures.

## 1 Introduction

The AcubeSAT nanosatellite is designed by SpaceDot, a non profit, interdisciplinary student research team in the Aristotle University of Thessaloniki (AUTH), to serve an open-source biological mission, under the auspices of the “Fly Your Satellite!” 3 programme of the ESA Education Office. The scientific output of the mission consists of images of microorganisms, captured by the on-board microscope and camera setup, in order to study their response to radiation and microgravity. The downlink of the scientific data, even though they will be compressed, sets strict requirements for the Communications Subsystem, due to the limited communication windows and power restrictions. In this paper, the design and testing of the Communications board will be presented.

## 2 Subsystem Description

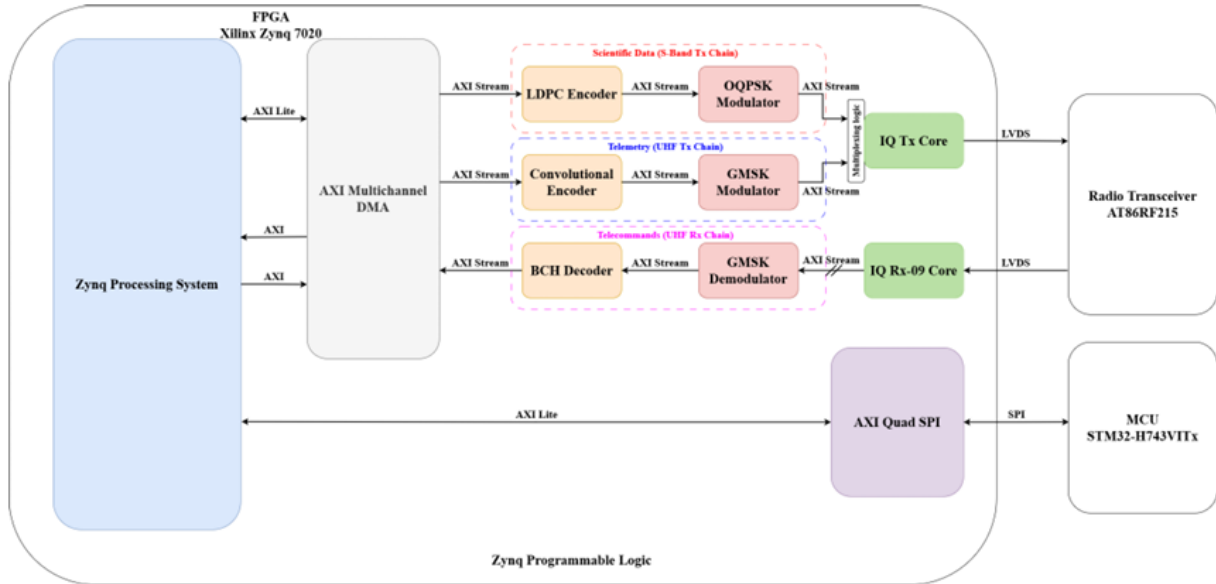
The novel biological experiment and the environmental conditions in Low Earth Orbit (LEO), have posed several challenging requirements to the definition of the telecommunications sub system, which all reflect on the design and testing approaches to be discussed. The AcubeSAT communications subsystem consists of two in-house designed antennas, a UHF deployable turn stile antenna and an S-Band patch antenna both designed in-house [7] and the COMMS Board, which this paper is going to expand upon.

The AcubeSAT COMMS Board is an in-house modified version of the SatNOGS COMMS hardware, designed by Libre Space Foundation [13], featuring in-house software and hardware IP cores. It is designed around an STM32H743 microcontroller unit that coordinates the sensors, RF circuitry, power supply unit and inter-board communication, a AC7Z020 SoM featuring an XC7Z020 FPGA SoC that is responsible for the generation of the modulated baseband signals along with their encoding and an AT86RF215 RF transceiver module that up-converts the FPGA modulated samples. The hardware differences with the original

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SatNOGS COMMS are mainly related to a better compatibility with the AcubeSAT mission in terms of power consumption, RF circuitry and mechanical properties (design changes in connector placement and the EMI shield design) [18].



**Figure 1:** FPGA Physical Layer System Architecture

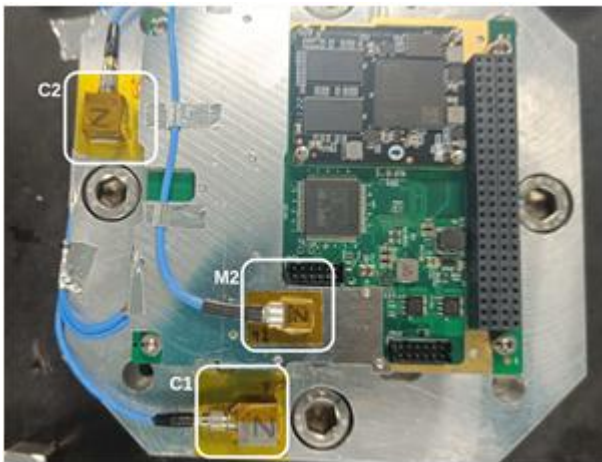
The in-house software design consists of the following main components: the MCU firmware [17], built around the STM32 HAL and the FreeRTOS kernel [1] for real-time task scheduling, the CCSDS data link layer module [14], implementing the CCSDS TM and TC Space Data Link standards [9, 8] and the physical layer module [16], hosting the error correction, modulation and synchronization algorithms. The specifications of the codes, modulations and data packet formats used are thoroughly described in [6]. The integration and testing philosophy of all on-board software is described in [11].

Furthermore, regarding the physical layer, the main task the team has taken is to transfer the majority of the algorithms to the on-board FPGA to increase performance and data throughput. A significant hindrance in implementing the entirety of the physical layer on FPGA is its significant power consumption, which comes in contrast to the limited power generation capabilities of a 3U LEO CubeSat. For this reason, the power footprint of each IP core is the primary metric used for optimization during design. In addition, apart from power simulations and testing in ambient conditions, the power footprint shall be closely monitored in flight representative conditions as described in the following section. All in all, the block diagram of the in-house FPGA IP Cores is shown in Figure 1.

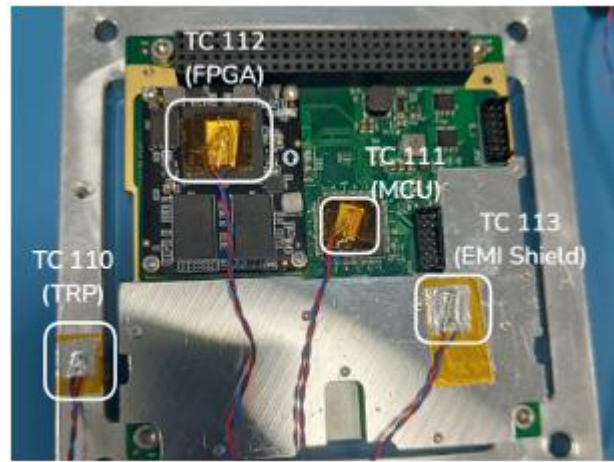
At the time of writing, three of the IP Cores have been fully developed and tested [15], including an OQPSK modulator, an LDPC encoder [12] and a BCH Decoder. It shall be noted that the configuration that was environmentally validated in the testing campaign included solely the OQPSK Tx chain. This choice is deemed acceptable as during an orbital pass, one Tx channel will be used at a time (UHF with GMSK or S-band with OQPSK), and S-band transmission has the highest power footprint on the board, thus simulating the worst scenario possible.

### 3 Environmental Testing and Validation

An environmental testing campaign is the means of testing the readiness of the subsystem to be sent to flight as a part of the whole satellite system and be space-qualified. These tests follow the philosophy “Test as you fly, fly as you test” [19], consisting of vibration sequences that mimic the launch mechanical stresses, followed by multiple Thermal Vacuum Chamber (TVAC) cycles, to test against the thermal cycles the CubeSat is going to endure in orbit. Being part of the FYS!3 programme enabled the team to utilize the CubeSat Support Facility at the ESA Education Office, ESEC-Galaxia, Transinne, Belgium, to conduct the aforementioned tests. The environmental testing campaign of AcubeSAT’s Communications Board was conducted in July 2024.



**Figure 2:** Accelerometers placed on the COMMS Board (VIBE Test)



**Figure 3:** Thermocouples placed on the COMMS Board (TVAC Test)

The vibration testing sequence consisted of the following per axis: modal searches, to identify the resonant modes of the board, a random vibration sequence to simulate the launch mechanical stresses (adhering to the GEVS profile [2]) and a second post-stress modal search to detect any system mode deviation from the previous search. Any significant changes to the modes may propose permanent mechanical alteration of the system, and are included in the pass/fail criteria of the test. This sequence is conducted for all axis X, Y and Z and the test data are correlated with FEM simulations conducted beforehand [5]. The three axes sequences were successfully completed, apart from a minor non-conformance that was issued after the posttest visual inspection. Notably, 2 Surface-mount Technology (SMT) standoffs, on which the FPGA daughter board was mounted, were slightly detached from the main board due to the mechanical stress induced upon them. Eventually, this had no impact on the functionality of the board, as no electrical interface was damaged, verified by the post-vibration full functional test and the TVAC tests that followed. Finally, the vibration test was considered successful, with the minor non-conformance formally issued to ESA with a proposed rework for the flight model that ensures the stability of the mechanical interface.

For the second phase, after installing the thermocouple sensors, as seen in Figure 3, to monitor the temperatures of the board, a total of four thermal cycles were run, including 1 non-operational and 3 operational cycles as per [10], after defining the minimum and maximum operational target temperatures of the chamber at -25 °C and 42 °C respectively [4]. These were chosen in order to mitigate the overheating of the FPGA, which was noticed during an initial thermal balance test to have an increased temperature

gradient on power-on even in ambient conditions. To further accommodate for this issue, a more time-restricted testing approach, representative of the operational time of the downlink chain in orbit, was employed. Specifically, 8 minutes were chosen to account for a best-case pass and 4 minutes for a nominal pass, as also shown in [3]. A collective summary of all the thermal cycles can be seen in Figure 4, where the thermocouple measurements over time are plotted.

The functional testing approach during TVAC consists of two functional modes. These are the reduced functionality mode tests throughout the cycling, simulating the "Idle" state on which the communications subsystem will be when there is no line-of-sight contact with the ground station, and the full functionality mode tests that are conducted at the cold and hot temperature plateaus, to simulate the "Tx/Rx" state during a ground station communication window. The plateaus refer to the constant temperature dwell sequences in the maximum and minimum operational temperatures after each thermal half-cycle. The full functional tests are conducted there in order to test the performance of the system under the most unfavorable conditions. In Figure 4 the plateaus for the first non-operational cycle are evident. For the next three operational cycles the dwells also showcase temperature spikes in certain thermocouples (e.g. TC-112 mounted on the FPGA), due to heating during the full functional test.

In terms of functionality, no issues were identified during the hot plateaus and the board performance was well within operational requirements. During the cold plateaus, some issues emerged initially, which the team promptly analyzed. The primary issue was that high inrush current caused the over-voltage protection circuits to be triggered in colder temperatures, thus disabling the powering on of the board. The issue was overcome by altering the power-on sequence of the board components via firmware and the rework was tested rigorously to verify the reliability of the power supply circuitry during colder temperatures. Therefore, after the rework, the following thermal cycles progressed nominally and the Communications Board performance was validated throughout them.

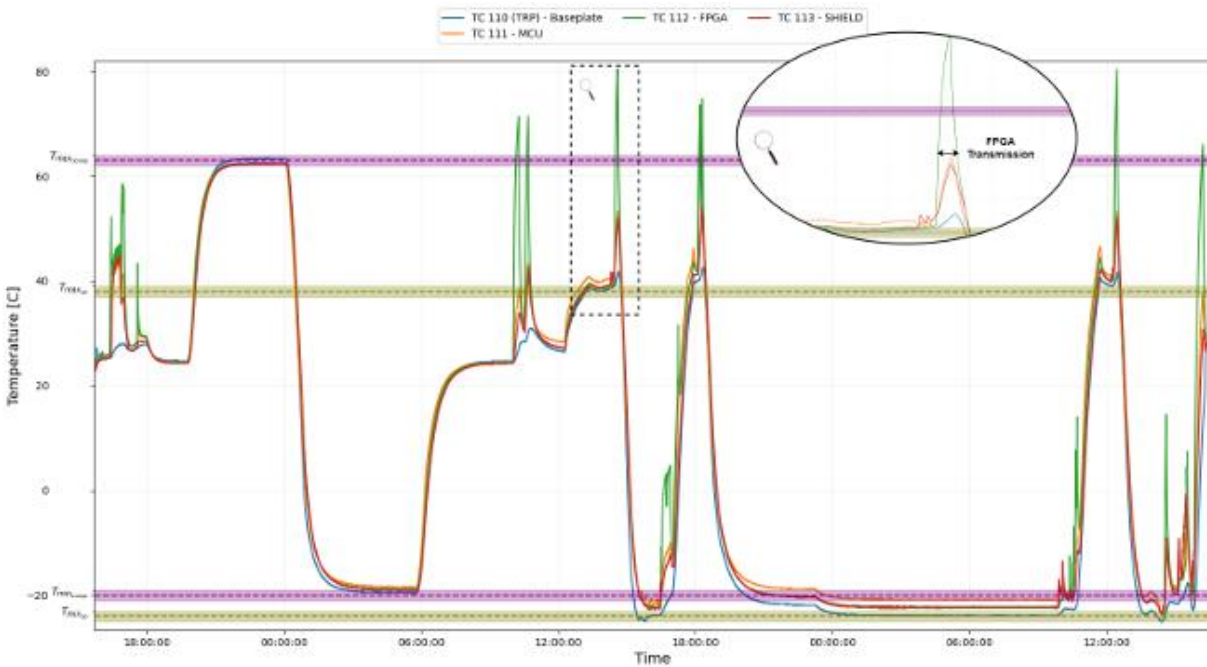


Figure 4: TVAC thermocouple data plotted over time

## 4 Conclusions

In conclusion, the environmental test of the AcubeSAT communications module was successful, and the subsystem is now considered qualified in thermal cycle and vibration testing, achieving a TRL-7 (Technology Readiness Level) status. Some future directions currently include continuing the FPGA IP Core development to include more modulation and encoding schemes and integrating the communication module with the rest of the system on a FlatSat level, before the CubeSat assembly, verifying the implementation of the data layer and operational procedures architecture on a system level. Finally, the environmental qualification of the hardware, described in this paper, and the ongoing software integration verification, establish the reliability of this mission-critical component in space conditions.

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