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Design and Electromagnetic Analysis of Interconnects in Silicon Interposer

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Abstract

In the post-Moore era, novel technologies are developed to support higher speeds, with significant emphasis in the field of advanced packaging. One of the technologies in this domain is 2.5D integration, where one or more chiplets are interconnected in the same substrate, called interposer. This integration technology allows for the chiplets to be placed in the same package, and thus the interconnects are much shorter than if the chiplets are placed in separate packages, resulting in lower interconnect latency. In this paper, signal integrity issues for a typical interposer that connects two dies are investigated. Three different types of interconnects are investigated. The metrics used to compare signal integrity among the three configurations are the reflection coefficient, insertion loss, coupling coefficient, and near- and far-end crosstalk between two differential interconnect pairs.

1 Introduction

Recently, the scaling of transistors has slowed down, due to thermal, technological, and economical limits. However, modern applications require continuously larger computing power and speed, emphasizing the need for novel integration techniques. One of these technologies lies in the area of advanced packaging and is called 2.5D integration, briefly described in the following section.

2 2.5D Integration

In traditional packaging, a semiconductor die is placed in a single package and the packages of different integrated circuits are connected on the Printed Circuit Board (PCB). The delay and power increase because the length of the traces that connect two different ICs on a PCB are in the millimeter scale. 2.5D integration is a more advanced technique, in which two or more semiconductor dies can be juxtaposed in the same package [6] - [10]. The dies are placed on top of a special substrate called an interposer, on which the connections between the dies are fabricated. An interposer is called passive if no active devices are contained in the substrate.

The connections on the interposer have a much shorter length, which introduces a smaller delay than in traditional 2D integration and, also, a lower power consumption. 2.5D integration has the advantage of reduced congestion when routing signals on the PCB. Furthermore, it enables heterogeneous integration, which means that dies of different technologies can be integrated in the same package, thus integrating e.g., high speed digital logic with analog circuits and power or telecommunication electronics.

3 Interposer topologies

A passive silicon interposer has been designed using the GPDK45 library provided by Cadence, as well as the Virtuoso software. The PDK provides 11 available metals, of which the top four are used for signal routing. On the top metal (M11), rectangular 40 µm X 40 µm pads are placed for each chiplet, so that the chiplets can be attached to the pads using a flip-chip technology. For each chiplet, 16 pads are used in a 4x4 configuration. The pitch between the pads is 40 µm. The pitch between the corresponding pads of the two different chiplets is 3.2 mm. The inner column of each pad array is used for signal routing, using two differential pairs of signals. The other 12 pads are used as ground pads. The pads and the connectivity for die1 can be seen in Fig. 1. The ground plane configuration and the traces connecting the chiplets differ in the three configurations that are investigated in the following sections.

The operating data rate of the circuit is assumed to be at 2 Gbps, which corresponds to a 1 GHz baseband frequency, plus the first harmonic taken into account, thus reaching a 2 GHz bandwidth. The nominal operating voltage is at 1 V with each single-ended signal fluctuating from -0.5 V to 0.5 V. The maximum acceptable voltage drop for the signals is 10% of the nominal Vdd, such that the high level of the signals must be at least 0.4 V [4].

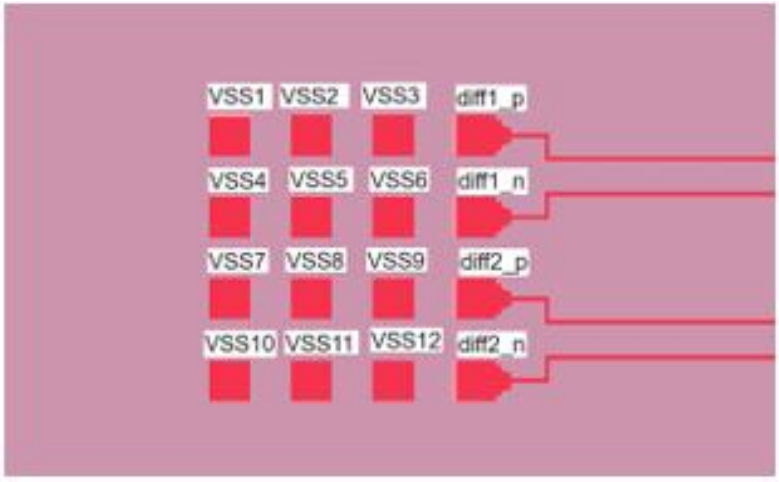

Figure 1: Interposer die1 pads

3.1. Interposer topologies

The simplest configuration for the interconnects is the microstrip line [11], [12]. The traces are placed on M11 in differential pairs and a continuous ground plane is placed on M8. The microstrip is easy to manufacture, and uses minimal space on the chip, since the signal traces do not require any guard traces. For this reason, no congestion to other signals is caused, but the drawback is that it does not offer any shielding between the two pairs, resulting in non-negligible crosstalk between the signal lines. The configuration is shown in Fig. 2.

Figure 2: Microstrip line topology

The geometric properties of the microstrip are chosen to match the differential impedance of both pairs to 100 Ω, using available tools [1]. The trace thickness and dielectric height are parameters given by the technology used. The trace width t and differential spacing s can be varied to achieve the desired impedance of 100 Ω.

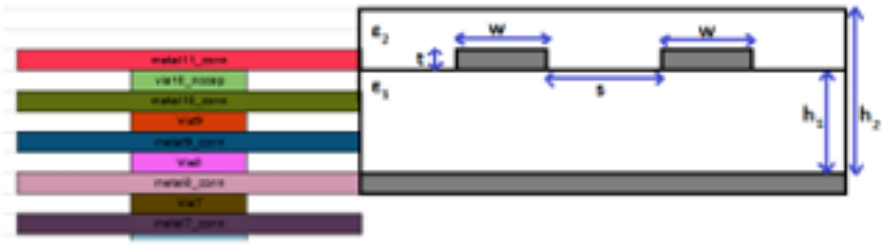

Figure 3: Microstrip line cross section

Parameter	Value
h_1 (μm)	3.50
h_2 (μm)	6.30
ε_1	3.99
ε_2	5.63
t (μm)	1.40
w $(\mu\mu)$	54.17
s (μm)	30.16
Z_d (Ω)	100.03

Table 1: Microchip parameters

The design is analyzed in HFSS 3D Layout, using a setup with a mesh frequency at 2 GHz, and an interpolating sweep from 0 to 15 GHz with a 20 MHz step. The simulation also models the skin effect inside the conductors. The results for the microstrip are listed in Table 4.

3.2. Coplanar waveguide

The second configuration investigated is the coplanar waveguide. The waveguide resembles the microstrip, but the differential pairs are placed in between ground traces also placed on M11. These ground traces are wider than the signal traces and provide sufficient capacitive shielding between the differential pairs by blocking the electric field lines from one pair to the other [5], [11], [12].

The geometric characteristics are again chosen for appropriate impedance matching, using typical formulae [2]. These characteristics are reported in Table 2.

Parameter	Value
h (μm)	3.50
ε	4.32
t (μm)	1.40
w ($\mu\mu$)	5.59
s (μm)	20.00
d (μm)	5.00
Z_d (Ω)	100.05

Table 2: Coplanar waveguide parameters

The results for the coplanar waveguide are reported in Table 4. It can be seen that the reflection coefficient is lower than for the microstrip and the insertion loss is higher. Thus, signal transmission is better through the waveguide. The most important result is the crosstalk, which has been reduced by 55% for the near-end and 75% for the far-end, respectively.

3.3. Coplanar stripline

The last configuration explored is the coplanar stripline. The stripline resembles the coplanar waveguide, but the signal traces are now placed on M9 instead of M11. On M11, an additional ground plane is utilized for enhanced shielding. For impedance matching, there are no analytical equations, such that the Q2D tool has been used. The cross section of the transmission line is simulated, with the geometric characteristics varying. The chosen characteristics are the features that provide 50 Ω impedance (for the single ended trace) at 2 GHz. The geometric properties are listed in Table 3.

Parameter	Value
h (μm)	3.50
ε	4.32
t (μm)	1.40
w ($\mu\mu$)	2.60
s (μm)	20.00
d (μm)	5.00
w_{gs} (μm)	20.00
w_{gb} (μm)	109.80
Z_d (Ω)	100.05

Table 3: Coplanar stripline parameters

The results are reported in Table 4. The reflection coefficient has risen significantly in comparison to both of the previous configurations, while the insertion loss is reduced. This behavior can also be seen from the eye diagram, where the positive voltage has dropped below the acceptable limit of 0.4 V. Thus, the signal propagation is not acceptable. The crosstalk has dropped by 63% for the near end and by 89% for the far-end. These results are better than the coplanar waveguide but come at the cost of poor signal propagation.

Parameter	Value		
	Microstrip	Coplanar waveguide	Coplanar stripline
Reflection coefficient (dB)	-16.29	-17.46	-10.23
Insertion loss (dB)	-1.46	-1.10	-3.19
NEXT coupling coefficient (dB)	-86.54	-93.1	-96.65
FEXT coupling coefficient (dB)	-94.03	-96.6	-100.69
Eye amplitude (mV)	865.66	898.26	783.77
Eye height (mV)	842.97	890.35	770.34
NEXT crosstalk (%)	0.043	0.019	0.016
FEXT crosstalk (%)	0.032	0.0078	0.0035

Table 4: Comparison of different interconnect structures

4 Comparison & Conclusions

Comparing the three configurations investigated, the microstrip is the simplest configuration but suffers the most from crosstalk between the differential pairs. In this case study, the crosstalk generated is still very low, but in larger applications with many signals placed adjacent to each other, this crosstalk can become significant and degrade normal operation. The coplanar waveguide offers very high shielding between the pairs and exhibits the best signal transmission characteristics out of the three configurations. The coplanar stripline can offer the best shielding but at the cost of poor transmission characteristics. Thus, the best choice between the three configurations is chosen to be the coplanar waveguide. The waveguide is also simpler to manufacture than the coplanar stripline, which makes this interconnect the most suitable choice.

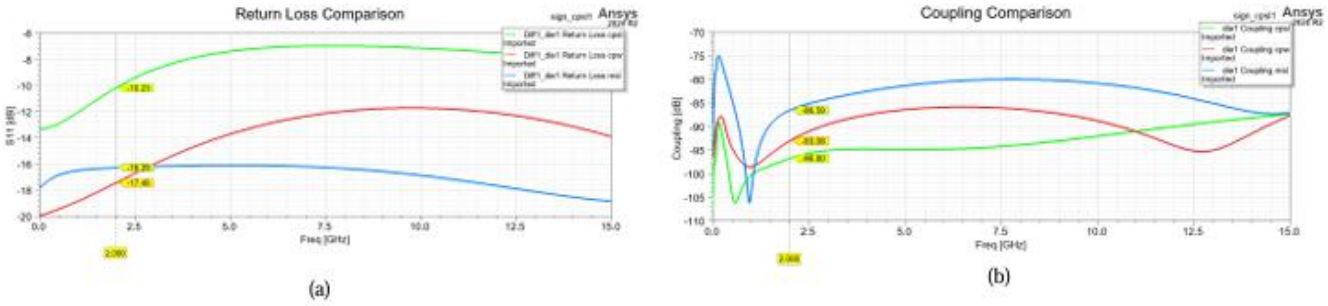

Figure 4: Return loss and coupling comparison

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