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Continuous and Symmetric Drain Current Compact Model for Nanoscale Triple-Gate FinFETs

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Abstract

In this work, we present a drain current compact model for nanoscale triple gate FinFETs satisfying continuity and source/drain symmetry. This is achieved by upgrading key equations of our original compact model. The formulated model is compact, valid in all regions of operation and its accuracy is validated through comparison with simulation data of nanoscale triple-gate transistor. The symmetry conditions are investigated and validated by performing the Gummel Symmetry Test.

Index Terms—Nanoscale triple-gate FinFETs, continuous and symmetric compact model.

1 Introduction

TRIPLE-GATE (TG) field-effect transistors (FETs) such as fin-shaped FETs (FinFETs) have been proposed for the 7 nm technology node and beyond [1], which exhibit excellent gate control for suppressing the short channel effects (SCEs) compared to the conventional planar MOSFETs [2], [3]. Generally, FinFETs are inherently symmetric devices and the source and drain contacts are interchangeable. Therefore, the compact models describing their behavior have to be electrically symmetric around the drain voltage of Vds = 0, a condition not usually satisfied.

The Gummel Symmetry Test (GST) was introduced as a benchmark test to qualify compact models developed for MOSFET circuit simulation and design [4], [5]. It has been demonstrated that a compact model can succeed to pass the GST when the potentials are referenced to the bulk [4], [6]. In the GST, the source and drain are driven in the opposite direction simultaneously by the applied voltage Vx. When Vx at the drain is swept from a negative to an equal positive value, the transistor under test is driven symmetrically from a reverse to a forward mode. In order to pass the GST, the symmetric drain current versus Vx plot must be an odd function and its nth order derivative should exist. One of the basic criteria used to decide the efficacy of a compact model is that the high-order derivatives of the drain current must be continuous at Vx = 0. Furthermore, the higher-order derivatives continuity implies that the second-order derivative should be equal to zero at Vx = 0.

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From the compact models developed for multiple-gate transistors, most of them examine the symmetry condition either for surface potential-based or charge-based compact models in independent-gate operation double-gate (DG) MOSFETs [7] or symmetric DG MOSFETs [8]-[13]. For the surface-potential based BSIM-CMG compact models in common-gate TG FinFETs presented in [14], [15], the symmetry condition has been examined in long-channel devices. For our charge-based compact model presented in [16] for nanoscale TG FinFETs, analogue gain-stage circuit was used for assessing its linear behavior, showing that the circuit's usable range is limited for input signal of power below about -15 dB. However, this compact model failed to pass the GST.

In this work, we update our previous drain current compact model for TG FinFETs [16] to a continuous and symmetric by modifying drastically the channel length modulation effect, the effective carrier mobility, the threshold voltage and the subthreshold swing coefficient, in a way satisfying the GST. The properly formulated initial charge-based compact model first is evaluated with simulation data in order to validate its efficiency. Then, the source/drain symmetry is verified by presenting high order derivatives of the drain current.

2 FORMULATION OF THE INITIAL COMPACT MODEL

The charge-based analytical compact model developed in our previous work [16] for TG FinFETs includes the SCEs, saturation velocity, source/drain series resistance and mobility degradation effects. For gate/source/drain potentials referenced to the bulk potential V_b [4], [6], the normalized inversion charge of the original model is formulated by the principal branch of the Lambert function W0(x) as follows:

$$q = W_0 e\left[e^{\frac{V_g - V_b - V_i - (V - V_b)}{2V_{th}}} \frac{e^{\frac{V_g - V_b - V_i - (V - V_S)}{2\eta V_{th}}}}{4e^{\frac{V_i + V_b - \Phi_1}{4e}} + e^{\frac{V_g - V_b - V_i - (V - V_b)}{2\eta V_{th}}}}\right] \tag{1}$$

where V_g is the gate voltage, V_t is the threshold voltage, V_{th} is the thermal voltage, V is the quasi-Fermi potential which varies from 0 at the source to V_{ds} at the drain, V_0 = 1 V represents a normalizing factor, η is the subthreshold swing coefficient, $V_{fb} = \Delta\varphi - \left(\frac{kT}{q}\right)\ln\left(\frac{N_A}{n_i}\right)$ is the flat-band voltage, Δφ is the gate work function referenced to silicon, N_A is the doping concentration of the silicon channel, ni is the intrinsic carrier concentration and c1 is a fitting parameter for adjusting the transition from the below to the above threshold region. The use of the Lambert function $W_0(x)$ in (1) allow us to exploit the function's inherent continuity in order to eliminate discontinuities and asymmetries by expressing key equations as a function of the normalized charge density. The following analytical approximation for the Lambert function $W_0(x)$ is used, with relative error less than 0.1% for wide range of positive x values:

$$W_0(x) = \frac{W_1(x)W_2(x)}{\sqrt{W_1^2(x) + W_2^2(x)}} \tag{2}$$

where

$$W_1(x) = (1 + 0.233878) \cdot \ln\left[\frac{12(x + 0.24)}{5\ln[2.4(x + 0.761034)]}\right] - 0.233878 \cdot \ln[2(x + 0.24)],$$

$$W_2(x) = x \tag{3}$$

In order to model the channel length modulation (CLM) effect, we originally included a mathematical smoothing function for the effective drain-source voltage ($V_{ds,eff}$) in our compact model that was valid in the saturation region, shortening the total length by a factor ΔL [16]. Performing the GST, while using this equation for $V_{ds,eff}$, leads to asymmetries because ΔL has a value only in the saturation region; otherwise it was fixed to zero. In general, a compact model has to include expression for $V_{ds,eff}$ that is inherently symmetric. In this work, we propose an alternative continuous function for ΔL in terms of the normalized inversion charge density to render the smoothing function symmetric and thus enable the compact model to pass the GST. In the forward mode operation (i.e. $V_{ds} > 0$ and $q_s > q_d$), the value of ΔL equivalent to that obtained using the $V_{d,eff}$ in [16] is

$$\Delta L_{eff} = \lambda_{av} \ln\left[1 + \frac{(V_d - V_s) - 2.2V_{th}(q_s - q_d)}{V_E}\right] \tag{4}$$

where λ_{eff} is the effective natural length of the TG FinFET, q_s and q_d are derived from (1) for $V = V_s$ and $V = V_d$, respectively and V_E is a fitting parameter. When the source and drain contacts are reversed (i.e. $V_{ds} < 0$ and $q_s < q_d$), ΔL will acquire in reverse mode a different value than that of the forward mode and as a result the model will be asymmetric. In order to bypass this issue, the expression (4) for ΔL is written as

$$\Delta L = \lambda_{eff} \ln\left[1 + \frac{V_{dn} - 2.2\left(\frac{V_d - V_s}{V_{dn}}\right)V_{th}(q_s - q_d)}{V_E}\right] \tag{5}$$

where

$$V_{dn} = \frac{\ln\left[1 + e^{100(V_d - V_s)} + e^{-100(V_d - V_s)}\right]}{100} \tag{6}$$

In relation (6), V_{dn} maintains positive value regardless of the source/drain reversal. In this way, the hyperbolic tangent contained in V_{dseff} of [16] is removed.

Moreover, it has been reported that asymmetries and discontinuities may also be introduced in a compact model because of the expression used for the effective carrier mobility (μ_{eff}) [17]. Following [18], μ_{eff} is analytically expressed in terms of the normalized inversion charge density q_0, allowing the compact model to satisfy the symmetry condition:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1 V_{th} q_0 + \theta_2 (V_{th} q_0)^2} \tag{7}$$

where μ_o is the low-field mobility, θ_1 and θ_2 are the mobility attenuation coefficients of first and second order, respectively and q_0 is described by the Lambert function $W_0(x)$

$$q_0 = W_0\left[\left(e^{\frac{V_g - V_b - V_t}{2V_{th}}}\right)\right] \tag{8}$$

The mobility attenuation coefficient θ_1, which includes the linear mobility attenuation coefficient $\theta_{1,0}$, the saturation velocity υsat and the series resistance R_{sd} [16], is expressed as a function of V_{dn} by:

$$\theta_1 = \theta_{1,0}\left[1 + \frac{\mu_0 V_{dn}}{v_{sat}(L - \Delta L)}\right] + \frac{\mu_0 W_{eff} C_{ox}}{L - \Delta L} R_{sd} \tag{9}$$

where $W_{eff} = 2H_{fin} + W_{fin}$ is the effective gate width of the TG FinFET, H_{fin} is the fin height and W_{fin} is the fin width. The mobility attenuation parameters μ_o, $\theta_{1,0}$, θ_2 and R_{sd} can be extracted using our new Y-function based methodology presented in [18].

Finally, performing the GST the impact of Vds on the threshold voltage Vt and the ideality coefficient η is taken into account. Following [16], the device parameters V_t and η are redefined in terms of V_{dn} by the analytical expressions

$$V_t = V_{fb} - \frac{A_1(V_{bi}+V_{dn})+A_2V_{bi}}{1-(A_1+A_2)} - \frac{V_{th}}{1-(A_1+A_2)}\ln\left[\frac{Q_nN_A}{n_i^2W_{fin}}\right] \tag{10}$$

$$\eta = \frac{1}{1-(A_1+A_2)} \tag{11}$$

where the built-in potential across the source/drain junctions is $V_{bi} = V_{th}\ln\left(\frac{N_DN_A}{n_i^2}\right)$ and N_D is the doping concentration of the source/drain contacts. The parameters Q_{th}, A_1 and A_2 presented in [16] are redefined through the modified drain source bias voltage V_{dn} in the minimum potential at the conductive path.

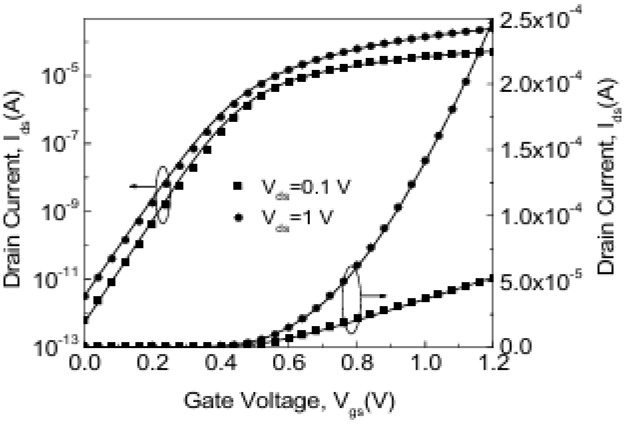

Fig. 1. Transfer characteristics in linear and semi-logarithmic representations of TG FinFET with dimensions L = 40 nm, Hfin = 20 nm, Wfin = 20 nm and tox = 1 nm. Symbols represent simulation data and solid lines the model results using the extracted model parameters: c1 =3, VE = 0.35 V, Vgc = 0.4 V, θ2 = 0, θ1,0 = 0.1 V-1, μ0 = 200 cm2/Vs, and Rsd = 125 Ω.

Our previous analytical drain current compact model [16], upgraded to a new compact model being continuous and symmetric by including the new modifications for ΔL, μ_{eff}, V_t and η presented in this work, is formulated as:

$$I_{ds} = W_{eff}\mu_{eff}C_{ox}(2V_{th})^2\left[\frac{q_s-q_d}{L} + \frac{1}{2}\frac{q_s^2-q_d^2}{L-\Delta L}\right] \tag{12}$$

The modified compact model (12) has been validated with simulation data of TG FinFET with channel length L = 40 nm, fin height H_{fin} = 20 nm, fin width W_{fin} = 20 nm, equivalent gate oxide thickness t_{ox} = 1 nm, doping concentration of silicon channel $N_A = 1.45 \times 10^{10}$ cm^{-3}, doping concentration of the source/drain contact regions $N_D = 10^{20}$ cm^{-3} and mid-gap gate metal work-function 4.71 eV corresponding to $\Delta\varphi = 0$ (i.e.$V_{fb} = 0$) [18]. The results of the validation are presented in Fig. 1. Using the extracted model parameters presented in the caption of Fig. 1, the agreement between simulation data and model results is very good.

3 THE GUMMEL SYMMETRY TEST

The model GST results for the TG FinFET of Fig. 1 were investigated with the gate/source/drain potentials referenced to zero bulk potential (Vb = 0). The inset of Fig. 2(a) shows the schematic of the GST circuit, where Vx is swept from -30 mV to +30 mV, while the gate voltage maintains a constant value. The model GST results for gate voltages Vg = 0, 0.25, 0.5 and 1 V, normalized to their absolute maximum values, are shown in Figs. 2(a)-2(d). It is evident that the derivatives of the modeled drain current up to the third order maintain continuity and symmetry around Vds = 0 for all gate voltages and the second derivative is zero at Vx = 0, validating the symmetric nature of the upgraded compact model.

4 CONCLUSION

In this work, we discuss certain formulations in our previous charge-based analytical drain current compact model for nanoscale TG FinFETs [16]. The new model is continuous and symmetric around $V_{ds} = 0$, verified by performing the Gummel Symmetry Test.

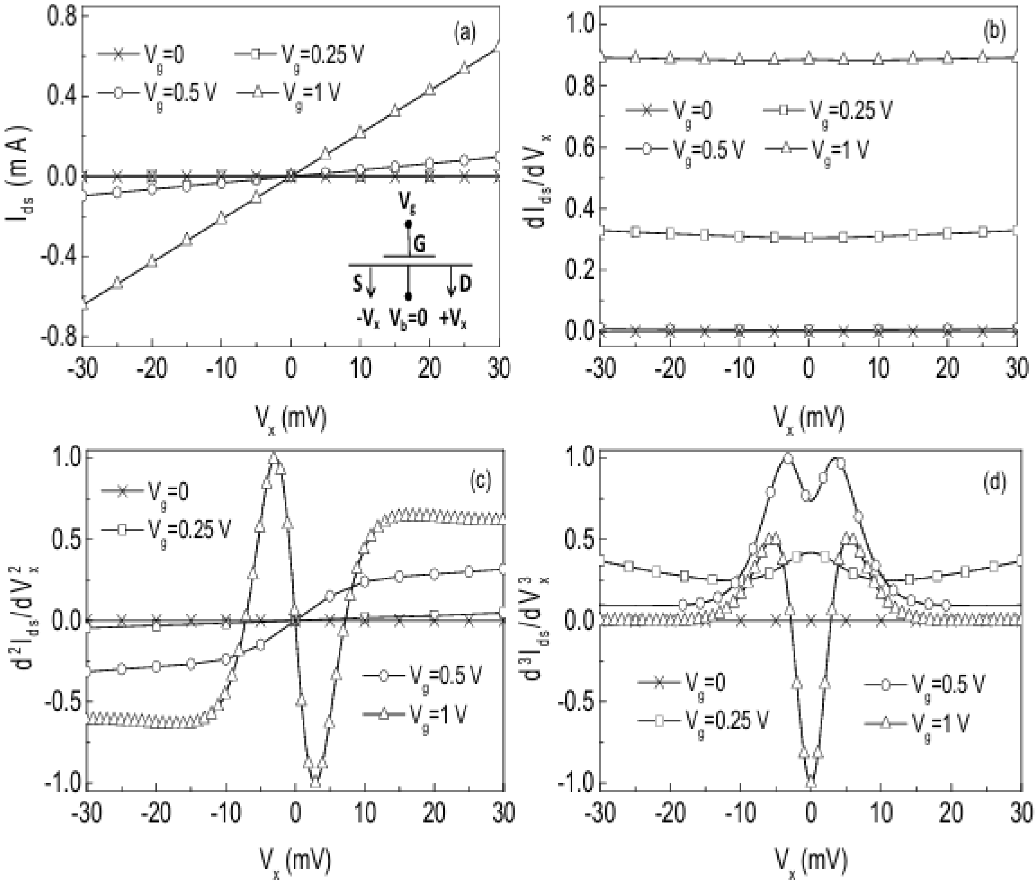

Fig. 2. Model GST results for derivatives of the drain current up to the third order at Vg = 0, 0.25, 0.5 and 1 V for TG FinFET with dimensions L = 40 nm, Hfin = 20 nm and Wfin = 20 nm. The current Ids(Vx) and its derivatives have been normalized to their absolute maximum values. The inset in Fig. 2(a) shows the schematic of the GST circuit.

The validation with simulated results, as well as the continuity and the symmetric nature of the formulated model, certify that it is suitable for implementation in circuit simulation tools.

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