EMERGING TECH CONFERENCE – Edge Intelligence

Volume 03, 2024, pages 160 – 165

Proceedings of Emerging Tech Conference: Edge Intelligence 2024

Automated Low-Noise Amplifier Design Methodology for Wireless Sensor Nodes

A. P. Tsimpou, A. Michailidis, V. Gogolou and T. Noulis

Electronics Laboratory, Physics Department, Aristotle University of Thessaloniki Thessaloniki Greece

ptsimpou@physics.auth.gr, anamicha@physics.auth.gr, vgogolou@physics.auth.gr, tnoul@physics.auth.gr

Abstract

This paper outlines a detailed design methodology for Low-Noise Amplifiers (LNAs), using a 65nm CMOS process node. The main target of this work is to simplify and accelerate the LNA design cycle without compromising on performance. The provided simulation results confirm the efficacy of the proposed methodology, deriving an LNA with S11<-30dB, S21>15dB, S12<-30dB, S22<-10dB, NF<3dB, at the specified frequency of 5 GHz.

1 Introduction

High-speed demands of mobile communication applications require high performance from the sub blocks of transceivers. Since the Low-Noise Amplifier (LNA) is usually the first block of the receiver chain, it dominates the Noise Figure (NF) of the system, hence it has the most impact on the overall sensitivity. LNAs can be found in receiver blocks of mobile communication applications SoC [1-2] and they are important to suppress the noise in the receiver and maintain an adequate signal-to-noise ratio. This attribute is derived from the input impedance matching of the LNA at the desired frequency of interest, which is a crucial specification with respect to the targeted application field [3].

The frequency that the LNA input impedance matches the source impedance (antenna) is the driving factor of the design flow and leads to specific design parameters of the LNA topology using the same node, e.g., the sizing of the input transistor and the integrated spiral inductor values [3]. Designing an LNA involves several critical challenges that impact its performance. These challenges include Noise Figure minimization and maximum power transfer, by achieving proper input and output impedance matching and high linearity to avoid distortion and ensuring stability across various frequencies and operating conditions [4].

2 LNA Analysis and the Proposed Design Methodology

2.1. Input Impedance Matching

The input impedance matching of an LNA is crucial for maximizing power transfer between the source and the amplifier while minimizing wave reflections back to the antenna. This is particularly important in Radio Frequency (RF) circuits, where any impedance mismatch can lead to significant power loss and degrade the overall system performance. The characteristic impedance of an antenna, which is typically connected to the input of the LNA block, is 50 Ohm. Therefore, it is essential to match the input impedance Zin of the

LNA to 50 Ohm. To obtain the input impedance matching criteria, small signal analysis was applied.

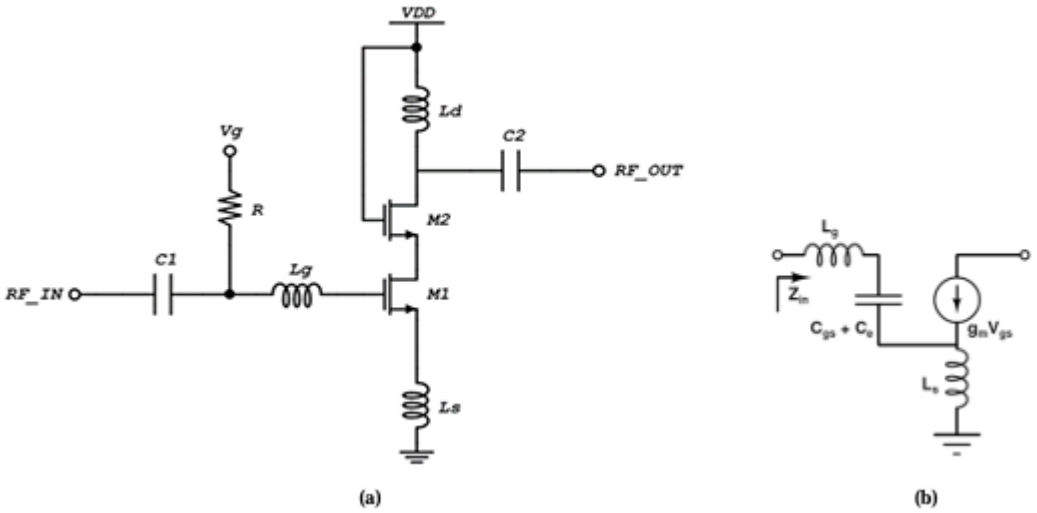


Figure 1: (a) Common Source LNA circuit topology (b) Small signal equivalent of the input.

The input impedance of the LNA with respect to the gate and degeneration inductors is extracted as follows [3],

$$Z_{in} = \frac{u_{in}}{i_{in}} = j\omega L_g + \frac{u_s + u_{gs}}{i_{in}}, \quad u_{gs} = \frac{i_{in}}{j\omega C_{gs}} \tag{1}$$

Where us is the source voltage and u_{gs} is the gate-source voltage of input transistor, while iin is the input current. The source current can be obtained as [3]:

$$i_s = i_{in} + g_m u_{gs} = i_{in}\left(1 + \frac{g_m}{j\omega C_{gs}}\right) \tag{2}$$

Where g_m is the transconductance of the input transistor M1. From the above equation the source voltage u_s is derived as [3]:

$$u_s = i_{in}\left(1 + \frac{g_m}{i\omega C_{gs}}\right) \cdot j\omega L_s \tag{3}$$

Combining (1), (2) and (3) we can get the following expression for the input impedance [3]:

$$Z_{in} = \frac{g_m \cdot L_s}{c_{gs}} + j\left[\omega\left(L_s + L_g\right) - \frac{1}{\omega C_{gs}}\right] \tag{4}$$

$$Re\{Z_{in}\} = \frac{g_m \cdot L_s}{c_{gs}} \tag{5}$$

To effectively match the input impedance of the LNA to 50 Ohm, the real part of Zin should be equal to 50 Ohm, while the imaginary part should be zero. Therefore, from (4) occurs the following equation for the frequency [3]:

$$Im\{Z_{in}\} = 0 \implies \omega(L_s + L_g) - \frac{1}{\omega C_{gs}} = 0 \implies \omega = \sqrt{\frac{1}{C_{gs}(L_s+L_g)}} \quad (6)$$

2.2. Noise Figure (NF)

Noise Factor is defined as the input signal-to-noise ratio divided by the output signal-to-noise ratio. For an amplifier, it can also be interpreted as the amount of noise introduced by the amplifier seen at the output, besides that which is caused by the noise of the input signal [5].

$$NF = \frac{SNR_{in}}{SNR_{our}} \quad (7)$$

For ideal transmission the LNA does not introduce any noise ($SNR_{in} = SNR_{our}$) and NF=1. For real systems:

$$NF = 1 + \frac{Y}{2} + \frac{Z_{11}}{Z_{11}+\omega^2 L_s^2 g_m} \quad (8)$$

Where γ is the factor related to the channel thermal noise of the MOSFET, gm is the transconductance and Z_{11} is the input impedance of the LNA. Hence, the noise figure of the LNA also depends on how well the input impedance of the LNA matches the source impedance, thus achieving its minimum value for a specific input transistor sizing and biasing point.

2.3. Stability Factor (K_f)

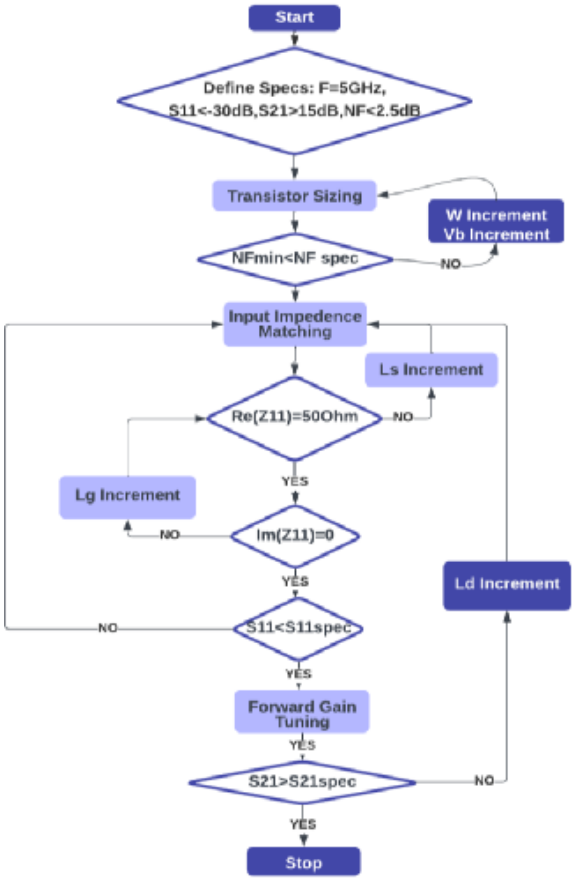
The stability factor (K_f) is a parameter, particularly used in RF and microwave designs, to determine whether an amplifier will oscillate under specific conditions. The LNA must remain stable for all source impedances at all frequencies. If the LNA begins to oscillate at any frequency, it becomes highly non linear, and its gain is very heavily compromised. The Kf for the LNA is obtained as follows [6] ,

$$K_f = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}||S_{21}|}, \quad \Delta = S_{11}S_{22} - S_{12}S_{21} \quad (9)$$

If $K_f > 1$, the amplifier is unconditionally stable, meaning it won't oscillate regardless of the source or load impedance.

2.4. LNA Design Methodology

The proposed design methodology is described via a flowchart illustrated in Figure 1. Also a pseudocode is provided to outline the design process. The workflow begins with defining the specifications for the LNA including the operating frequency (f), the input reflection coefficient (S_{11spec}), the forward gain (S_{21spec}) and the noise figure (NF_{spec}). The next step invloves transistor sizing: if the NF_{min} value is grater than NF_{spec}, there should be an increment at the transistor width (W) or the bias voltage Vb until the condition is satisfied. Once the NF specification is met, the process checks if the real part of the input impedance is equal to 50 Ohms. If not, the inductor Ls is incremented until Re(Z11) = 50. Then, the imaginary part of the input impedance is set to zero by increasing the value of inductor L_g. The input impedance matching procedures is repeated until $S_{11} \leq S_{11spec}$. The forward gain tuning process follows: if $S_{21} < S_{21spec}$, the value of the inductor Ld should be increased and the input impedance should be rematched to 50 Ohms. Finally, the forward gain tuning process is repeated until the specified forward gain is achieved



Algorithm 1: LNA Design Methodology

Define LNA Specifications and parameters:
Frequency → f
Input impedance → S_{11spec}
Forward Gain → S_{21spec}
Noise Figure → NF_{spec}
while ($NF_{min} > NF_{spec}$)
  {increase W; increase Vb;}
if ($NFmin \leq NF_{spec}$)
  {**return** W and Vb values; **break**;}
Input Matching Procedure:
while ($Re(Z_{11}) \neq 50$)
    {increase L_s;}
  if ($Re(Z_{11}) = 50$)
    {**return** L_s value; **break**;}
while ($Im(Z_{11}) \neq 0$)
    {increase L_g;}
  if ($Im(Z_{11}) = 0$)
    {**return** L_g value; **break**;}
if ($S_{11} > S_{11spec}$)
  {**goto** Input Matching Procedure;}
else if ($S_{21} < S_{21spec}$)
  {increase L_d;
  goto Input Matching Procedure;}
else {return L_d value;}
end;

Figure 2: Flowchart of the proposed design methodology with its respective pseudocode representation.

3 Methodology Verification and Simulation Results

The common source LNA topology that was designed using a 65nm CMOS process node is illustrated in figure 1(a). This LNA topology is commonly used in RF systems due to its ability to provide good input matching, gain and noise performance. The transistor M1 is the main amplifying device, and the RF signal is applied to its gate. The transistor M2 provides a stable bias current to M1, and it is used to improve the gain and the output impedance of the circuit, providing also isolation between input and output ports. Inductors Ls and Lg are essential for input impedance matching and the Ld is used as the output load and helps in maximizing the gain at the desired frequency. Finally, the capacitors C1, C2 are blocking the DC signal, and the resistor R is used for biasing the gate of M1, setting the operating point of the transistor. The device sizing, the supply and bias voltages and the inductor values, after applying the proposed design methodology at the targeted frequency of f = 5 GHz, are shown in Table 1. The physical design of the LNA is illustrated in Figure 3. The S-parameters, noise figure and stability factor post-layout simulations of the circuit are shown in Figures 4(a) and 4(b) respectively. The post-layout simulation performance metrics of the LNA are summarized in Table 2. Using the proposed process the defined specifications were met:

Parameter	Value
Frequency	5 GHz
VDD	1.2 V
Vg	550 mV
W/L (M1)	275 um / 0.06 um
W/L (M2)	390 um / 0.08 um
Lg	3 nH
Ls	170 pH
Ld	2.4 pH

Table 1: Device sizing, supply and bias voltages and inductor values of the LNA design derived from the proposed methodology

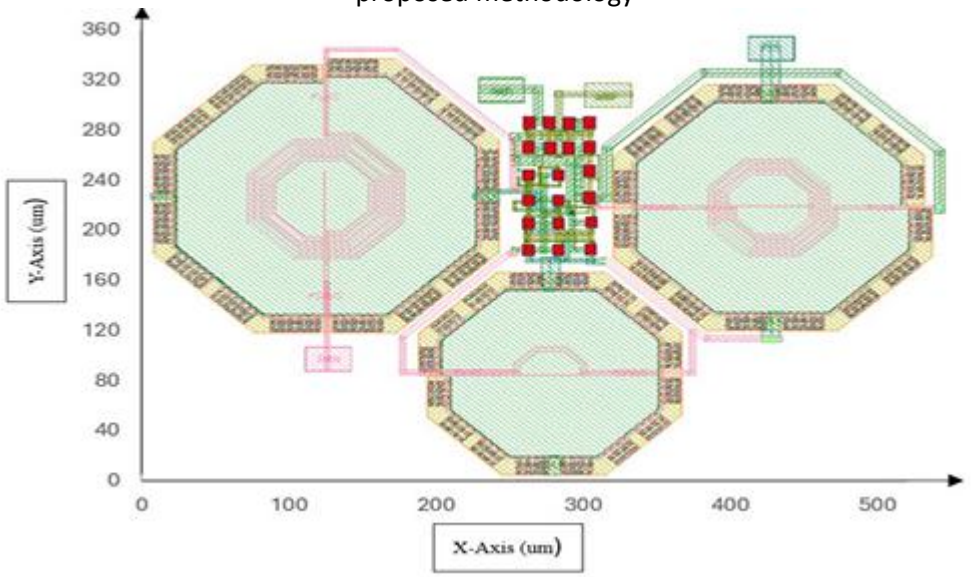


Figure 3: Physical Design of the designed LNA.

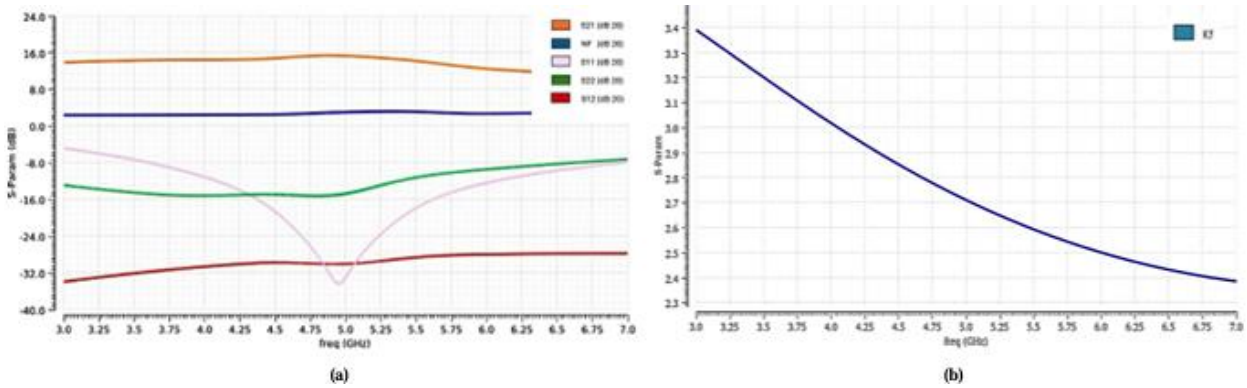


Figure 4: (a) S-Parameters and Noise Figure post-layout simulation (b)Stability Factor KF post-layout stimulation.

LNA Performance Metrics @ 5GHz	Value
S11	-32 dB
S21	15.2 dB
S12	-30.5 dB
S22	-15 dB
NF	2.6 dB
Power Consumption	22 mW
Silicon Area	0.19 mm2

Table 2: Post-layout simulation results of the designed LNA using the proposed methodology.

4 Conclusion

The common source LNA topology circuit, that was designed using the proposed methodology met successfully the given specifications, proving its efficiency while providing competitive LNA designs in an accelerated manner. The approach provides a structured framework for designers, making the design of LNAs more efficient and accessible without compromising on key performance metrics.

5 Acknowledgement

“This work was supported by the DAAD-Projekt 57647733 Radiation-Hard Integrated Circuits Educational platform ”RADHARD”, with funds from the Federal Foreign Office and German Academic Exchange Service (Deutscher Akademischer Austauschdienst) in the framework of the ”Hochschulpartnerschaften mit Griechenland 2023 2025” action.”

References

[1] A. Madan, M. McPartlin, C. Masse, W. Vaillancourt, and J. Cressler, "A 5 GHz 0.95 dB NF Highly Linear Cascode Floating-Body LNA in 180 nm SOI CMOS Technology," IEEE Microwave and Wireless Components Letters, vol. 22, 2012.

[2] C. Li, O. El-Aassar, A. Kumar, M. Boenke, and G. M. Rebeiz, "LNA Design with CMOS SOI Process 1.4dB NF K/Ka band LNA," in Proceedings of the 2018 IEEE/MTT-S International Microwave Symposium-IMS, Philadelphia, PA, USA, 10–15 June 2018, pp. 1484–1486.

[3] C. Sad, A. Michailidis, T. Noulis, and K. Siozios, "A Hybrid GA/ML-Based End-to-End Automated Methodology for Design Acceleration of Wireless Communications CMOS LNAs," Electronics, vol. 12, no. 2428, 2023. doi: 10.3390/electronics12112428.

[4] H. A. Eshghabadi and F. Eshghabadi, "Design Considerations for Low Noise Amplifier," in IEEE International Conference on Circuits and Systems (ICCAS), 2012.

[5] A. Dao, "Integrated LNA and Mixer Basics," National Semiconductor Application Note AN-884, April 1993.

[6] S. Kassim and F. Malek, "Microwave FET amplifier stability analysis using Geometrically-Derived Stability Factors," 2010 International Conference on Intelligent and Advanced Systems, Kuala Lumpur, Malaysia, 2010, pp. 1-5, doi: 10.1109/ICIAS.2010.5716171.